

# MAC-PHY INTERFACE SPECIFICATION



*Making High-Speed Wireless A Reality ...*

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# 1 Introduction

This document describes the interface between implementations of the WIMEDIA PHY and a MAC. The interface is intended for applications where the MAC resides on a separate chip from the PHY and may also be useful as an internal interface or macrocell interface.

Section 4 defines the interface signals, their directions and functions.

Section 5 defines the interface parameters and registers. A recommended mapping for PHY parameters is provided along with the register map for PHY registers and setup and hold timing for register access.

Section 6 defines the frame formats for data exchanges over the interface.

Section 7 is the Theory of Operation for the complete interface covering the PHY states and transitions, reset and sleep protocols, frame timing references, preamble control and transmit and receive operations for both single frame and burst mode operation as well as receive error cases. The section is completed by definition of the CCA and Management interface protocols.

There are two appendices to this specification. Appendix A provides an Electrical Interface and Appendix B defines formats for two WiMedia managed identifiers.

## 1.1 REFERENCED DOCUMENTS

- [1] Multiband OFDM Physical Layer Specification, Release 1.0, April 27th 2005
- [2] WIMEDIA MAC Layer Technical Specification, Version 0v98
- [3] Multiband OFDM Physical Layer Specification, Release 1.0, April 27th 2005, Section 7.2 Channelization
- [4] Multiband OFDM Physical Layer Specification, Release 1.0, April 27th 2005, Section 7.3 Physical Layer Timing
- [5] Multiband OFDM Physical Layer Specification, Release 1.0, April 27th 2005, Section 10.2 Ranging reference signal
- [6] Multiband OFDM Physical Layer Specification, Release 1.0, April 27th 2005, Section 10.5 Ranging Calibration Constants
- [7] WIMEDIA MAC Layer Technical Specification, Version 0v98, Annex C

## 2 Notational Conventions

The use of the word *shall* is meant to indicate a requirement which is mandated by the standard, i.e. it is required to implement that particular feature with no deviation in order to conform to the standard. The use of the word *should* is meant to recommend one particular course of action over several other possibilities, however without mentioning or excluding these others. The use of the word *may* is meant to indicate that a particular course of action is permitted. The use of the word *can* is synonymous with is able to – it is meant to indicate a capability or a possibility.

All floating-point values have been rounded to 4 decimal places.

## 3 Abbreviations and Acronyms

BM	BURST MODE
CCA	CLEAR CHANNEL ASSESSMENT
CRC	CYCLIC REDUNDANCY CODE
ETSI	EUROPEAN TELECOMMUNICATIONS STANDARDS INSTITUTE

FCC	FEDERAL COMMUNICATIONS COMMISSION
FCS	FRAME CHECK SEQUENCE
FFI	FIXED-FREQUENCY INTERLEAVING
HCS	HEADER CHECK SEQUENCE
LQI	LINK QUALITY INDICATOR
LSB	LEAST-SIGNIFICANT BIT
MAC	MEDIUM ACCESS CONTROL
MBOA	MULTIBAND OFDM ALLIANCE
MIFS	MINIMUM INTERFRAME SPACE
MSB	MOST SIGNIFICANT BIT
OFDM	ORTHOGONAL FREQUENCY DIVISION MODULATION
PHY	PHYSICAL (LAYER)
PLCP	PHYSICAL LAYER CONVERGENCE PROTOCOL
PPM	PARTS PER MILLION
PT	PREAMBLE TYPE
RSSI	RECEIVED SIGNAL STRENGTH INDICATOR
RX	RECEIVE OR RECEIVER
SIFS	SHORT INTERFRAME SPACE
TF	TIME-FREQUENCY
TFC	TIME-FREQUENCY CODE
TFI	TIME-FREQUENCY INTERLEAVING
TX	TRANSMIT OR TRANSMITTER
UWB	ULTRA WIDEBAND

4 INTERFACE SIGNAL DESCRIPTION

The MAC-PHY signal interface is depicted in Figure 4-1. It consists of the Data Interface including an 8-bit data bus, the Control Interface, the CCA Interface and the Management Interface. The Data Interface, which is used to transfer data to and from the MAC, operates differently depending on the state of the PHY. The Control Interface is used by the MAC to control the operating state of the PHY and by the PHY to indicate TX/RX status to the MAC. The CCA Interface is used for Clear Channel Assessment status indication. The Management Interface is used to access the PHY registers.

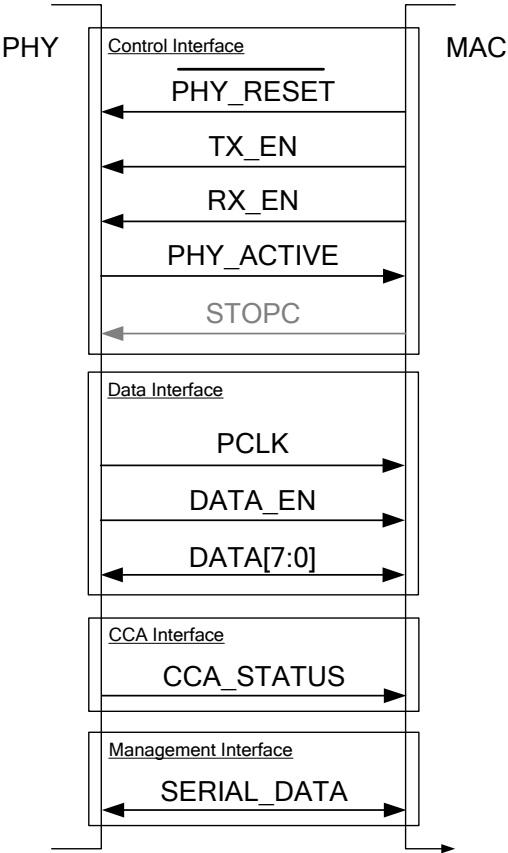


Figure 4-1 PHY-MAC interface signals

Table 4-1, Table 4-2, Table 4-3 and Table 4-4 define the signals in the Control Interface, Data Interface, CCA Interface and Management Interface, respectively. The operational mode of the Data Interface in each PHY state is summarized in Table 4-5.

## 4.1 INTERFACE SIGNAL DEFINITIONS

### 4.1.1 CONTROL INTERFACE

*Table 4-1 Control Interface Signals*

SIGNAL	WIDTH (BITS)	DIR	DESCRIPTION
!PHY_RESET	1	MAC to PHY	<p>!PHY_RESET is asserted for PHY specific interval PHYResetTime to clear all PHY variables and reset the PHY to its initial state. The PHY writes STANDBY to PMMODE and transitions to STANDBY state after !PHY_RESET is de-asserted and reset operations have completed.</p> <p>!PHY_RESET is asynchronous to PCLK.</p> <p>!PHY_RESET is ACTIVE LOW</p>
TX_EN	1	MAC to PHY	<p>TX_EN is used to place the PHY in 'TRANSMIT' State. [Its secondary use (with RX_EN) is to transition from SLEEP to STANDBY when the PHY clock source has been stopped for power saving.]</p> <p>TX_EN is synchronous to PCLK except in SLEEP state.</p> <p>TX_EN is ACTIVE HIGH.</p>
RX_EN	1	MAC to PHY	<p>RX_EN is used to place the PHY in RECEIVE State. [Its secondary use (with TX_EN) is to transition from SLEEP to STANDBY when the PHY clock source has been stopped for power saving.]</p> <p>RX_EN is synchronous to PCLK except in SLEEP state.</p> <p>RX_EN is ACTIVE HIGH.</p>
PHY_ACTIVE	1	PHY to MAC	<p>PHY_ACTIVE is used by the PHY to indicate that it is either transmitting or receiving a frame over the air. In 'TRANSMIT' state, the rising edge of PHY_ACTIVE indicates the start of frame at the local antenna and the falling edge indicates that the entire frame has been transmitted over the air. In RECEIVE state, the rising edge of this signal indicates that the start of the preamble has been detected (SyncDelay + the preceding synchronization fields earlier) and the falling edge indicates that the entire frame has been received (PHYActiveDelay earlier) at the local antenna. PHY_ACTIVE is also used in the special cases of Exit from SLEEP and RESET.</p> <p>PHY_ACTIVE is synchronous to PCLK.</p> <p>PHY_ACTIVE is ACTIVE HIGH.</p>
STOPC (optional)	1	MAC to PHY	<p>On/Off signal for PCLK in STANDBY state. PCLK is active when STOPC is de-asserted and not active when STOPC is asserted.</p> <p>STOPC is asynchronous to PCLK.</p> <p>STOPC is ACTIVE HIGH.</p>

### 4.1.2 DATA INTERFACE

*Table 4-2 Data Interface Signals*

SIGNAL	WIDTH (BITS)	DIR	DESCRIPTION
PCLK	1	PHY to MAC	Interface clock provided by the PHY. Interface signals are synchronous to the rising edge of PCLK (see Appendix A).  The nominal rate of PCLK is 66MHz.
DATA_EN	1	PHY to MAC	In TRANSMIT state, this signal is used by the PHY to request more data from the MAC. In RECEIVE state, it is used to indicate to the MAC that there is valid data on the DATA[7:0] bus.  DATA_EN is synchronous to PCLK.  DATA_EN is ACTIVE HIGH.
DATA[7:0]	8	Bi-directional	DATA[7:0] is an 8-bit wide data bus driven by the MAC in TRANSMIT state and by the PHY in all other states including SLEEP.  DATA[7:0] is synchronous to PCLK whether driven by the PHY or the MAC.  DATA[7:0] '1' is HIGH.

### 4.1.3 CCA INTERFACE

*Table 4-3 CCA Interface Signals*

SIGNAL	WIDTH (BITS)	DIR	DESCRIPTION
CCA_STATUS	1	PHY to MAC	The PHY returns CCA_STATUS after a CCA request is initiated by the MAC writing to the CCRE register via SERIAL_DATA.  CCA_STATUS is synchronous to PCLK.  CCA_STATUS is ACTIVE HIGH.

### 4.1.4 MANAGEMENT INTERFACE

*Table 4-4 Management Interface Signals*

SIGNAL	WIDTH (BITS)	DIR	DESCRIPTION
SERIAL_DATA	1	Bi-directional	The MAC writes control and address bits to SERIAL_DATA to initiate register access.  Register access is initiated by the MAC with control and address bits. SERIAL_DATA is driven by the MAC for Write operations. It is driven by the MAC for control and address parts of Read operations and by the PHY for the data part of Read operations.  SERIAL_DATA is synchronous to PCLK.  SERIAL_DATA '1' is HIGH.

## 4.2 PHY OPERATIONAL STATE

*Table 4-5 PHY Readiness State*

STATE	DESCRIPTION
RESET	Transitional state in which the configuration parameters are reset to default values. PCLK is undefined (see 7.1.1)
SLEEP	The radio is off. PCLK is off (see 7.1.2)
STANDBY	The radio is off. PCLK is on (unless STOPC is asserted). STANDBY is a higher activity state than SLEEP
READY	Parts of the radio are on. PCLK is on
TRANSMIT	The PHY Tx paths and the radio transmit path are active. PCLK is on
RECEIVE	The PHY Rx paths and the radio receive path are active. PCLK is on



## 5 REGISTERS

Two sets of parameters are defined to allow the MAC to control the operation of the PHY and permit information to be provided by the PHY to the MAC.

- **STATIC Parameters**

These parameters are fixed for a given instantiation of the MAC and PHY. They can be considered to be constants for the purposes of the definition of the MAC-PHY Interface and their values can be defined in a given PHY data sheet, stored as constants in the system implementation or provided by any other means. The static parameters are defined in Table 5-1.

- **DYNAMIC Parameters**

These parameters may be changed during operation of the system, and affect operation of the PHY. They shall be implemented within the PHY as registers and can be read and/or written (depending on the specific parameter) via the Serial Management Interface. The dynamic registers are defined in Table 5-2.

### 5.1 BIT ORDERING AND INTERPRETATION

All data structures, except where explicitly stated, are defined with the bit order as shown in Figure 5-3.

Reserved bits shall be ignored on reading and set to '0' on writing.

### 5.2 REGISTER ADDRESS SPACES

The PHY has 256 addressable 8-bit registers (8-bit address, 8-bit data) divided into 3 regions:

- 1) Dynamic Register region defined by this specification : address 00(h)~1F(h)
- 2) Optional Static Parameter region defined by this specification : address 20(h)~7F(h)
- 3) Vendor Specific Register region for vendor defined registers : address 80(h)~FF(h)

## 5.3 STATIC PARAMETER DEFINITIONS

*Table 5-1 Description of Static Parameters*

REGISTER	OCTETS	DEFINITION																								
SupportedRegDomains	2	Supported regulatory domains. Bit set ‘1’ if supported, ‘0’ otherwise  First Octet <table><tr><th><u>Bit</u></th><th><u>Domain</u></th></tr><tr><td>[2:0]</td><td>Reserved</td></tr><tr><td>[3]</td><td>European Telecommunications Standards Institute (ETSI)</td></tr><tr><td>[4]</td><td>Federal Communication Commission (FCC)</td></tr><tr><td>[5]</td><td>Industry Canada (IC)</td></tr><tr><td>[6]</td><td>Association of Radio Industries and Business (ARIB)</td></tr><tr><td>[7]</td><td>Ministry of Information and Communication (MIC) (Korea)</td></tr></table> Second Octet <table><tr><th><u>Bit</u></th><th><u>Domain</u></th></tr><tr><td>[7:0]</td><td>Reserved</td></tr></table>	<u>Bit</u>	<u>Domain</u>	[2:0]	Reserved	[3]	European Telecommunications Standards Institute (ETSI)	[4]	Federal Communication Commission (FCC)	[5]	Industry Canada (IC)	[6]	Association of Radio Industries and Business (ARIB)	[7]	Ministry of Information and Communication (MIC) (Korea)	<u>Bit</u>	<u>Domain</u>	[7:0]	Reserved						
<u>Bit</u>	<u>Domain</u>																									
[2:0]	Reserved																									
[3]	European Telecommunications Standards Institute (ETSI)																									
[4]	Federal Communication Commission (FCC)																									
[5]	Industry Canada (IC)																									
[6]	Association of Radio Industries and Business (ARIB)																									
[7]	Ministry of Information and Communication (MIC) (Korea)																									
<u>Bit</u>	<u>Domain</u>																									
[7:0]	Reserved																									
SupportedDataRates	2	Set of supported data rates. Bit set ‘1’ if supported, ‘0’ otherwise  <table><tr><th><u>Bit</u></th><th><u>Data Rate Supported</u></th></tr><tr><td>[0]</td><td>53.33Mbps</td></tr><tr><td>[1]</td><td>RESERVED</td></tr><tr><td>[2]</td><td>80Mbps</td></tr><tr><td>[3]</td><td>106.67Mbps</td></tr><tr><td>[4]</td><td>RESERVED</td></tr><tr><td>[5]</td><td>160Mbps</td></tr><tr><td>[6]</td><td>200Mbps</td></tr><tr><td>[7]</td><td>320Mbps</td></tr><tr><td>[8]</td><td>400Mbps</td></tr><tr><td>[9]</td><td>480Mbps</td></tr><tr><td>[15:10]</td><td>RESERVED</td></tr></table>	<u>Bit</u>	<u>Data Rate Supported</u>	[0]	53.33Mbps	[1]	RESERVED	[2]	80Mbps	[3]	106.67Mbps	[4]	RESERVED	[5]	160Mbps	[6]	200Mbps	[7]	320Mbps	[8]	400Mbps	[9]	480Mbps	[15:10]	RESERVED
<u>Bit</u>	<u>Data Rate Supported</u>																									
[0]	53.33Mbps																									
[1]	RESERVED																									
[2]	80Mbps																									
[3]	106.67Mbps																									
[4]	RESERVED																									
[5]	160Mbps																									
[6]	200Mbps																									
[7]	320Mbps																									
[8]	400Mbps																									
[9]	480Mbps																									
[15:10]	RESERVED																									
NumChannelsSupported	1	Number of supported channels																								
SupportedDiversity	1	Number of additional antennas provided for diversity  <table><tr><td>[1:0]</td><td>Number of receive antennas</td></tr><tr><td>[3:2]</td><td>Reserved</td></tr><tr><td>[5:4]</td><td>Number of transmit antennas</td></tr><tr><td>[7:6]</td><td>Reserved</td></tr></table>	[1:0]	Number of receive antennas	[3:2]	Reserved	[5:4]	Number of transmit antennas	[7:6]	Reserved																
[1:0]	Number of receive antennas																									
[3:2]	Reserved																									
[5:4]	Number of transmit antennas																									
[7:6]	Reserved																									

SupportedChannels	1	Supported Channels. Bit set '1' if supported, '0' otherwise.  <div> <div>Bit</div> <div>Channel Supported</div> </div> [0] TFC channels in band group 1 supported [1] TFC channels in band group 2 supported [2] TFC channels in band group 3 supported [3] TFC channels in band group 4 supported [4] TFC channels in band group 5 supported Bits [7:5] RESERVED
TXPowerLevel	16	Array of transmit power levels.  Each element from 0 to (NumTxPowerLevels-1) of the array holds a supported transmit power. The format of the power level datum is PHY vendor specific. The other elements shall be set to 0.  Element 0 shall be the maximum transmit power supported.
NumTxPowerLevels	1	Number of transmit power levels supported. Permitted range (0..15) with 0 meaning a single fixed power level only.  [3:0] – number of levels (permitted range 0..15) [7:4] – RESERVED
SupportedPHYStates	1	Supported PHY States. Bit set '1' if supported, '0' otherwise.  [0] SLEEP [1] STANDBY [2] READY [3] TRANSMIT [4] RECEIVE Bits [7:5] RESERVED.
PHYClockAccuracy	1	Accuracy of PHY clock. Units ppm.
PHYResetTime	1	Interval during which !PHY_RESET shall be held asserted for the PHY to perform RESET operation. Units us.
WakeUpDelay	2	Time to transition from SLEEP mode to STANDBY mode. Units 0.5 us
TurnOnDelay	2	Radio turn-on time during transition from STANDBY mode to READY mode. Units 0.5 us.
TxDataDelay	1	Delay, not greater than 4us, before the end of the preamble at the local antenna before which the PHY will not assert DATA_EN to request the first octet of header data. (See 7.4.)  Units us
TxDelay	2	Delay from the rising edge of TX_EN to the time when the PHY feeds the leading edge of the preamble waveform to the antenna. Units: ns.

RxDelay	2	Delay from the rising edge of RX_EN to the time when the PHY begins the preamble acquisition processing. Units ns.
Tx2RxDwellTime	2	Minimum interval between PHY_ACTIVE de-assertion (in TRANSMIT State) and RX_EN assertion. Units ns.
Rx2TxDwellTime	2	Minimum interval between RX_EN de-assertion and TX_EN assertion. Units ns.
SyncDelay	2	<p>Delay from the end of the last symbol of the Frame Synchronization Sequence of the preamble waveform in the local antenna to the time when the PHY asserts PHY_ACTIVE.</p> <p>Note that since the preamble arrives asynchronously with respect to PCLK, PHY vendors should provide this value for the shortest amount of time before PHY_ACTIVE could be asserted assuming optimal alignment of the received preamble and PCLK.</p> <p>Units ns</p>
TxSetupTime	2	<p>Minimum time between setting of transmit control registers and assertion of TX_EN.</p> <p>Units PCLK cycles.</p>
RxSetupTime	2	<p>Minimum time between setting of receive control registers and the assertion of RX_EN or de-assertion of PHY_ACTIVE.</p> <p>Units PCLK cycles.</p>
TxHoldTime	2	<p>Minimum time between the assertion of TX_EN and changing transmit control registers for the next frame.</p> <p>Units PCLK cycles.</p>
RxHoldTime	2	<p>Minimum time between the assertion of RX_EN or deassertion of PHY_ACTIVE and changing receive control registers for the next frame.</p> <p>Units PCLK cycles.</p>
PHYID	2	PHY identifier to specify vendor, product and version. See Appendix B for format and coding
PHYVersion	1	Version number of WiMedia PHY specification supported. See Appendix B for format and coding
PHYActiveDelay	2	<p>Delay from the end of the last symbol of the frame received in the local antenna and PHY_ACTIVE de-assertion.</p> <p>Note that since received frames arrive asynchronously with respect to PCLK, PHY vendors should provide this value for the shortest amount of time before PHY_ACTIVE could be de-asserted assuming optimal alignment of the received frame and PCLK.</p> <p>Units ns</p>
CCAValidTime	1	<p>Interval following MAC setting CCRE = '1' after which PHY should respond with CCA measurement result.</p> <p>Units 0.5μs</p>

MinPTChangeLength	1	Minimum MAC Frame Payload length for the preamble type of the next frame to be different to the current frame.  Fixed value = 1 octet
RangingSupported	1	Support of ranging  [0] - Set to '1' if supported otherwise set to '0' [1] – support for 528MHz precision (Mandatory) [2] – support for 1056MHz precision [3] – support for 2112MHz precision [4] – support for 4224MHz precision [5] – support for RANGINGTIMER [23:16] [6] – support for RANGINGTIMER [31:24] [7] RESERVED
RANGING_TRANSMIT_DELAY	2	See Referenced Documents [6] for the definition of RANGING_TRANSMIT_DELAY  Units 1/4224 MHz - same as RANGINGTIMER (see Table 5-2)
RANGING_RECEIVE_DELAY	2	See Referenced Documents [6] for the definition of RANGING_RECEIVE_DELAY  Units 1/4224 MHz - same as Ranging Timer (see Table 5-2)

## 5.4 STATIC PARAMETER CODING

If the values of the static parameters are stored in the PHY, they should be implemented as read only values using the addresses and formats shown in Figure 5-1 and Figure 5-2.

	bit-7			bit-4	bit-3		bit-0
7F(h)	Reserved						
7E(h)	Reserved						
7D(h)	Reserved						
7C(h)	Reserved						
60(h)	Reserved						
5F(h)	TxPowerLevel15						
5E(h)	TxPowerLevel[15:0]						
5D(h)	TxPowerLevel0						
5C(h)	TxPowerLevel[0:0]						
50(h)	TxPowerLevel[0:0]						
4F(h)	Reserved						
4E(h)	Reserved						
4D(h)	RxHoldTime[15:8]						
4C(h)	RxHoldTime[7:0]						
4B(h)	TxHoldTime[15:8]						
4A(h)	TxHoldTime[7:0]						
49(h)	RxSetupTime[15:8]						
48(h)	RxSetupTime[7:0]						
47(h)	TxSetupTime[15:8]						
46(h)	TxSetupTime[7:0]						
45(h)	SyncDelay[15:8]						
44(h)	SyncDelay[7:0]						
43(h)	RxDelay[15:8]						
42(h)	RxDelay[7:0]						
41(h)	TxDelay[15:8]						
40(h)	TxDelay[7:0]						

Figure 5-1 Static Parameter Encoding 40(h) - 7F(h)

	bit-7			bit-4	bit-3			bit-0
3F(h)				RANGING_RECEIVE_DELAY[15:8]				
				RANGING_RECEIVE_DELAY				
3E(h)				RANGING_RECEIVE_DELAY[7:0]				
3D(h)				RANGING_TRANSMIT_DELAY[15:8]				
				RANGING_TRANSMIT_DELAY				
3C(h)				RANGING_TRANSMIT_DELAY[7:0]				
3B(h)				Rx2TxDwellTime[15:8]				
				Rx2TxDwellTime				
3A(h)				Rx2TxDwellTime[7:0]				
39(h)				Tx2RxDwellTime[15:8]				
				Tx2RxDwellTime				
38(h)				Tx2RxDwellTime[7:0]				
37(h)				TurnOnDelay[15:8]				
				TurnOnDelay				
36(h)				TurnOnDelay[7:0]				
35(h)				WakeUpDelay[15:8]				
				WakeUpDelay				
34(h)				WakeUpDelay[7:0]				
33(h)				PHYActiveDelay[15:8]				
				PHYActiveDelay				
32(h)				PHYActiveDelay[7:0]				
				TxDataDelay				
31(h)				TxDataDelay[7:0]				
				MinPTChangeLength				
30(h)				MinPTChangeLength[7:0]				
				CCAValidTime				
2F(h)				CCAValidTime[7:0]				
				PHYResetTime				
2E(h)				PHYResetTime[7:0]				
				PHYClockAccuracy				
2D(h)				PHYClockAccuracy[7:0]				
				RangingSupported				
2C(h)	Reserved	32 Bit	24 Bit	4224MHz	2112MHz	1056MHz	528MHz	Ranging Supportec
				SupportedPHYStates				
2B(h)	Reserved			RECEIVE	TRANSMIT	READY	STANDBY	SLEEP
				NumTxPowerLeve				
2A(h)				NumTxPowerLevel[7:0]				
				SupportedChannels				
29(h)	Reserved			TFC BG5	TFC BG4	TFC BG3	TFC BG2	TFC BG1
				SupportedDiversity				
28(h)	Reservec	TxDiversity[5:4]		Reservec		RxDiversity[1:0]		
				NumChannelsSupported				
27(h)				NumChannelsSupported[7:0]				
				SupportedDataRates2				
26(h)	Reserved						480Mb/s	400Mb/s
				SupportedDataRates1				
25(h)	320Mb/s	200Mb/s	160Mb/s	Reservec	106.67Mb/s	80Mb/s	Reserved	53.3Mb/s
				SupportedRegDomain2				
24(h)	Reserved							
				SupportedRegDomain1				
23(h)	MIC	ARIB	IC	FCC	ETSI	Reserved		
				PHYVersion				
22(h)				PHYVersion[7:0]				
				PHYID[15:8]				
21(h)				PHYID				
				PHYID[7:0]				
20(h)								

Figure 5-2 Static Parameter Encoding 20(h) - 3F(h)

## 5.5 DYNAMIC REGISTER DEFINITIONS

All registers in the Dynamic Register area are readable (R) and writable (W) by the MAC except RDY in the CONTROL register and RANGINGTIMER which are Read Only.

It is intended that the Current Regulatory Domain (CRD) register is not writable by a user application and can only be set by initialization or reset operations to ensure compatibility with regional regulatory requirements.

*Table 5-2 Description of Dynamic Registers*

ADDR.	REGISTER	R/W	DESCRIPTION	INIT.												
00(h)	CONTROL	R/W (Except RDY which is R)	PHY Control register [0] RDY - Result of !PHY_RESET. 0 = Normal completion of initialization 1 = Abnormal completion of initialization [1] Reserved [2] RNGEN 0 = RANGINGTIMER not set by PHY 1 = RANGINGTIMER set by PHY [3] CCRE – CCA Request 0 = Stop CCA estimation 1 = Start CCA estimation [7:4] RESERVED	0(h)												
01(h)	CRD	R/W	[2:0] RESERVED [7:3] CRD – Current regulatory domain Each domain is mapped to a bit in the register, as follows: <table><tr><td><u>Bit</u></td><td><u>Domain</u></td></tr><tr><td>3</td><td>European Telecommunications Standards Institute (ETSI).</td></tr><tr><td>4</td><td>Federal Communication Commission (FCC).</td></tr><tr><td>5</td><td>Industry Canada (IC).</td></tr><tr><td>6</td><td>Association of Radio Industries and Business (ARIB).</td></tr><tr><td>7</td><td>Association Ministry of Information and Communication (MIC) (Korea)</td></tr></table>	<u>Bit</u>	<u>Domain</u>	3	European Telecommunications Standards Institute (ETSI).	4	Federal Communication Commission (FCC).	5	Industry Canada (IC).	6	Association of Radio Industries and Business (ARIB).	7	Association Ministry of Information and Communication (MIC) (Korea)	0(h)
<u>Bit</u>	<u>Domain</u>															
3	European Telecommunications Standards Institute (ETSI).															
4	Federal Communication Commission (FCC).															
5	Industry Canada (IC).															
6	Association of Radio Industries and Business (ARIB).															
7	Association Ministry of Information and Communication (MIC) (Korea)															
02(h)	TXCHAN	R/W	[5:0] TXCH - Channel of next transmitted frame. [7:6] RESERVED  (Note: TXCH is coded as (3-bit Band Group   3-bit TFC) as defined in Referenced Documents [3] for the mapping of Channel Number to Band Group and TFC)	0(h)												



03(h)	TXCTL	R/W	<p>Transmit Control</p> <p>[0] TXPT – Preamble type of next transmitted frame. 0 = Standard Preamble 1 = Burst Preamble</p> <p>[1] Reserved</p> <p>[3:2] TXANT – Transmit antenna to be used. Value 0..SupportedDiversity[5:4] where: 00 identifies transmit antenna 1 01 identifies transmit antenna 2 10 identifies transmit antenna 3 11 identifies transmit antenna 4</p> <p>[7:4] TXPWR – Index into TxPowerLevels for transmit power level</p>	0(h)
04(h)	RXCHAN	R/W	<p>Receive Channel</p> <p>[5:0] RXCH - Channel of next received frame.</p> <p>[7:6] RESERVED</p> <p>(See Referenced Documents [3] for the mapping of Channel Number to Band Group and TFC)</p>	0(h)
05(h)	RXCTL	R/W	<p>Receive Control</p> <p>[0] RXPT - Preamble type of next received frame. 0 = Standard Preamble 1 = Burst Preamble</p> <p>[1] PTON (R/W) 0 = PHY does not process PT bit in PLCP header 1 = PHY does process PT bit in PLCP header</p> <p>[3:2] RXANT – Receive antenna to be used. Value 0..SupportedDiversity[1:0] where: 00 identifies receive antenna 1 01 identifies receive antenna 2 10 identifies receive antenna 3 11 identifies receive antenna 4</p> <p>[7:4] RESERVED</p>	0(h)
06(h)	PMMODE	R/W	<p>[2:0] Power management mode. Values: 0 READY. 1 STANDBY 2 SLEEP Values 3-7 RESERVED</p> <p>[7:3] RESERVED</p>	1(h)
07(h) – 0A(h)	RANGINGTIMER	R	<p>Ranging Timer (units 1/4224MHz)</p> <p>[31:0] RANGINGTIMER - 32-bit ranging counter value. Note that this register requires multiple read operations (07(h) to 0A(h)) to retrieve the full value.</p>	0(h)
0B(h)	CRDEExtension	R/W	<p>Extension for 2<sup>nd</sup> Octet of Regulatory domains</p> <p>[7:0] RESERVED</p>	0(h)

## 5.6 REGISTER MAP

Figure 5-3 shows the register map. Gray portions in the map are reserved.

	bit-7			bit-4	bit-3			bit-0
1F(h)	Reserved							
1E(h)	Reserved							
1D(h)	Reserved							
1C(h)	Reserved							
0B(h)	CRDEXTENSION							
0A(h)	RANGINGTIMER							
09(h)				RANGINGTIMER[31:24]				
08(h)				RANGINGTIMER[23:16]				
07(h)				RANGINGTIMER[15:8]				
06(h)				RANGINGTIMER[7:0]				
05(h)	PM							
04(h)	Reserved				PMMODE			
03(h)	RXCTL							
02(h)	Reserved				RXANT		PTON	RXPT
01(h)				RXCHAN				
00(h)	Reserved			RXCH				
7F(h)	TXCTL							
7E(h)	TXPWR			TXANT		Reserved	TXPT	
7D(h)	TXCHAN							
7C(h)	Reserved			TXCH				
7B(h)	CRD							
7A(h)		CRD			Reserved			
79(h)	CONTROL							
78(h)	Reserved				CCRE	RNGEN	Reserved	RDY

Figure 5-3 Register Map

## 5.7 REGISTER SET ACCESS TIMING

### 5.7.1 TRANSMIT CONTROL REGISTERS

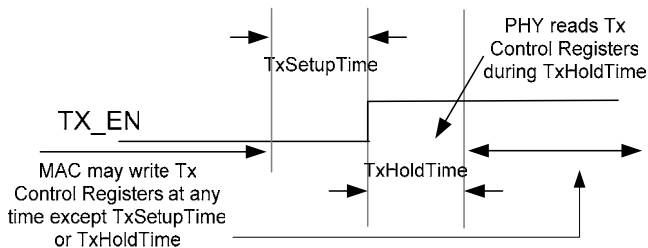
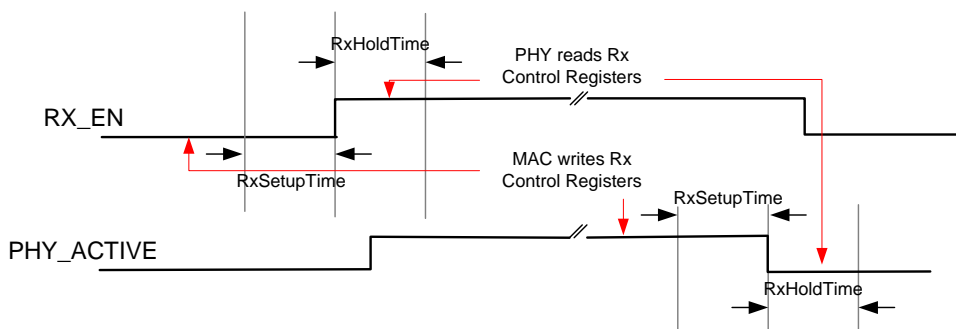


Figure 5-4 Transmit Control Register Setup & Hold

TXCHAN and TXCTL (TXPT, TXANT and TXPWR) are registers used to specify parameters for the next transmit frame operation. They shall be set by the MAC at least TxSetupTime PCLK cycles before the assertion of TX\_EN and are held stable for at least TxHoldTime PCLK cycles. The PHY shall read these registers within this TxHoldTime period. The values

of these registers then control the parameters for the transmit frame operation corresponding to this TX\_EN assertion.

### 5.7.2 RECEIVE CONTROL REGISTERS



*Figure 5-5 Receive Control Register Setup & Hold*

RXCHAN and RXCTL (RXPT and RXANT) are registers used to specify parameters for the next receive frame operation. They shall be set by the MAC at least RxSetupTime PCLK cycles before the assertion of RX\_EN and are held stable for at least RxHoldTime PCLK cycles. The PHY shall read these registers in this RxHoldTime period ignoring any PTON setting and any previous BM or PT settings. The values of these registers then control the parameters for the receive frame operation corresponding to this RX\_EN assertion.

For burst mode reception, the MAC shall set the registers for the next receive frame operation at least RxSetupTime PCLK cycles before PHY\_ACTIVE de-assertion indicating the end of frame reception. The PHY shall read the registers within RxHoldTime PCLK cycles following the de-assertion of PHY\_ACTIVE. These registers then control the parameters for the reception of the next frame if RX\_EN is not de-asserted. In receive burst mode (see 7.8.3) PTON together with the BM and PT bits of the preceding frame's PLCP header may override the RXPT register setting.

RX\_EN de-assertion and re-assertion has precedence over PHY\_ACTIVE de-assertion and will cause the PHY to overwrite any internal values loaded from the receive control registers.

*Table 5-3 Register Access Parameter Values*

PARAMETER	MINIMUM VALUE (PCLK PERIODS)	MAXIMUM VALUE (PCLK PERIODS)
TxSetupTime	0	128
TxHoldTime	0	128
RxSetupTime	0	128
RxHoldTime	0	128

## 6 FRAME STRUCTURES

According to the WiMedia PHY specification (Referenced Document [1]), data is transmitted and received least-significant bit first (bit zero octet zero ... bit 7 octet zero, bit 0 octet 1 ... bit 7 octet 1 etc.). Consequently, the PLCP header, as shown in Figure 6-2, is presented to DATA[7:0] as shown in Figure 6-1.

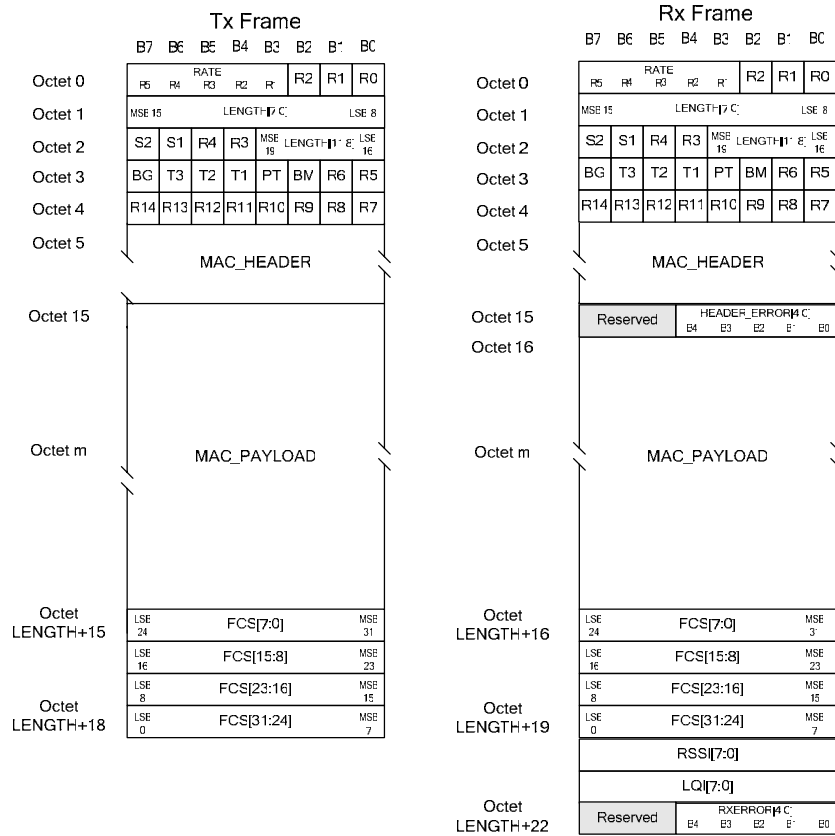


Figure 6-1 Frame Structures for Transmit & Receive States



Figure 6-2 PLCP Header Format

The MAC\_HEADER, MAC\_PAYLOAD and FCS are presented to the PLCP as defined in the WiMedia MAC specification (Referenced Document [2]). As defined in that specification, the coefficients ( $a_{31}.. a_0$ ) of the CRC result polynomial :

$$a_{31}X^{31} + a_{30}X^{30} + a_{29}X^{29} + a_{28}X^{28} + a_{27}X^{27} + \dots + a_7X^7 + a_6X^6 + a_5X^5 + a_4X^4 + a_3X^3 + a_2X^2 + a_1X + a_0$$

are mapped to the bits of the FCS as shown in Figure 6-3 and presented to the PLCP as shown in Figure 6-1.

bits: b31	b30	b29	...	b2	b1	b0
a0	a1	a2	...	a29	a30	a31

Figure 6-3 FCS Field format

Thus when presented to the PLCP least significant octet first (FCS[7:0]) the coefficients of the CRC are transmitted in the order  $a_{31}.. a_0$ .

The following TxFrame control bits (see Figure 6-2) shall be set by the MAC in all transmitted frames and shall be delivered to the MAC by the PHY in the RxFrame format of all received frames:

- RATE is the data rate at which the MAC Frame Payload is transmitted. If LENGTH = 0, RATE shall be set to '00000';
- LENGTH is the MAC Frame Payload length in octets excluding the FCS octets. If LENGTH is zero, the FCS field is not present;
- SCRAMBLER is set to zero during initialization of the PHY or after any !PHY\_RESET. The unsigned binary integer set in SCRAMBLER is incremented by the MAC, modulo 4, for each frame transmitted from the MAC to its PHY;
- BM and PT shall be set in all transmitted frames according to the rules defined in section 7.6;
- The MAC sets TX\_TFC and BG as derived from TXCHAN (see Table 5-2) in all transmitted frames.

Table 6-1 Tx Frame Fields

FIELD	BITS	DESCRIPTION																				
R0, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14	1	RESERVED bits  On 'TRANSMIT', RESERVED bits SHALL be set to zero																				
RATE	5	Indication of transmit data rate of MAC Frame Payload <table><tr><td>Rate (Mb/s)</td><td>R1-R5</td></tr><tr><td>53.3</td><td>00000</td></tr><tr><td>80</td><td>00001</td></tr><tr><td>106.7</td><td>00010</td></tr><tr><td>160</td><td>00011</td></tr><tr><td>200</td><td>00100</td></tr><tr><td>320</td><td>00101</td></tr><tr><td>400</td><td>00110</td></tr><tr><td>480</td><td>00111</td></tr><tr><td>Reserved</td><td>01000-11111</td></tr></table>	Rate (Mb/s)	R1-R5	53.3	00000	80	00001	106.7	00010	160	00011	200	00100	320	00101	400	00110	480	00111	Reserved	01000-11111
Rate (Mb/s)	R1-R5																					
53.3	00000																					
80	00001																					
106.7	00010																					
160	00011																					
200	00100																					
320	00101																					
400	00110																					
480	00111																					
Reserved	01000-11111																					
LENGTH	12	Length of MAC Frame Payload (unit: octet)  12-bit unsigned binary integer lsb 8 --- msb 19																				
SCRAMBLER	2	Scrambler initialization bits S1 and S2																				

BM	1	<div>Burst Mode bit (Interframe Space following this frame)</div> <div>0 = Normal Mode (SIFS or other)</div> <div>1 = Burst Mode (MIFS)</div> <div>(Note :</div> <div>SIFS = pSIFS</div> <div>MIFS = pMIFS</div> <div>as defined in Referenced Documents [4])</div>																		
PT	1	<div>Preamble type of the frame following this frame</div> <div>0 = Standard Preamble</div> <div>1 = Burst Preamble</div>																		
TX_TFC	3	<div>TF Code used at the transmitter</div> <table><tr><td>TF Code</td><td>T1-T3</td></tr><tr><td>1</td><td>100</td></tr><tr><td>2</td><td>010</td></tr><tr><td>3</td><td>110</td></tr><tr><td>4</td><td>001</td></tr><tr><td>5</td><td>101</td></tr><tr><td>6</td><td>011</td></tr><tr><td>7</td><td>111</td></tr><tr><td>Reserved</td><td>000</td></tr></table>	TF Code	T1-T3	1	100	2	010	3	110	4	001	5	101	6	011	7	111	Reserved	000
TF Code	T1-T3																			
1	100																			
2	010																			
3	110																			
4	001																			
5	101																			
6	011																			
7	111																			
Reserved	000																			
BG	1	<div>Least-significant bit of the BAND GROUP used at the transmitter</div> <table><tr><td>Band Group</td><td>BG</td></tr><tr><td>1, 3, 5</td><td>1</td></tr><tr><td>2, 4</td><td>0</td></tr></table>	Band Group	BG	1, 3, 5	1	2, 4	0												
Band Group	BG																			
1, 3, 5	1																			
2, 4	0																			
MAC_HEADER	80	MAC Frame header																		
MAC_PAYLOAD	---	Frame Data																		
FCS	32	Frame FCS																		

Table 6-2 Rx Frame Fields

FIELD	BITS	DESCRIPTION
R0, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14	1	RESERVED bits On RECEIVE, RESERVED bits SHALL be ignored
RATE	5	Same as Tx Frame Fields
LENGTH	12	Same as Tx Frame Fields

SCRAMBLER	2	Scrambler initialization bits (S1 and S2) shall be ignored on receive.
BM	1	<p>Burst Mode bit indicates the Inter-Frame Space following this receive frame</p> <p>0 = Normal IFS (Depends on MAC context)</p> <p>1 = Burst Mode IFS (MIFS)</p> <p>(Note :</p> <p>SIFS = pSIFS</p> <p>MIFS = pMIFS</p> <p>as defined in Referenced Documents [4])</p>
PT	1	<p>Preamble Type for the frame following this frame</p> <p>0 = Standard Preamble</p> <p>1 = Burst Preamble</p>
TX_TFC	3	Same as Tx Frame Fields
BG	1	Same as Tx Frame Fields
MAC_HEADER	80	Same as Tx Frame Fields
HEADER_ERROR	5	<p>Immediate Header Error reporting. Error is indicated by the corresponding bit set to 1.</p> <p>bit 0: RESERVED</p> <p>bit 1: RESERVED</p> <p>bit 2: RESERVED</p> <p>bit 3: UNSUPPORTED_RATE</p> <p>bit 4: HCS_ERROR</p> <p>All bits = "0" represents "NO_ERROR"</p>
MAC_PAYLOAD	---	Same as Tx Frame Fields
FCS	32	Same as Tx Frame Fields
RSSI	8	Receive power estimate of received signal
LQI	8	Quality estimate of received signal
RXERROR	5	<p>Receiving results of Rx frame</p> <p>Each bit represents the cause of error</p> <p>bit 0: PAYLOAD_ERROR</p> <p>bit 1: RESERVED</p> <p>bit 2: RESERVED</p> <p>bit 3: UNSUPPORTED_RATE</p> <p>bit 4: HCS_ERROR</p> <p>All bits = "0" represents "NO_ERROR"</p>

## 7 INTERFACE THEORY OF OPERATION

### 7.1 OVERVIEW

A simplified PHY state diagram is shown in Figure 7-1.

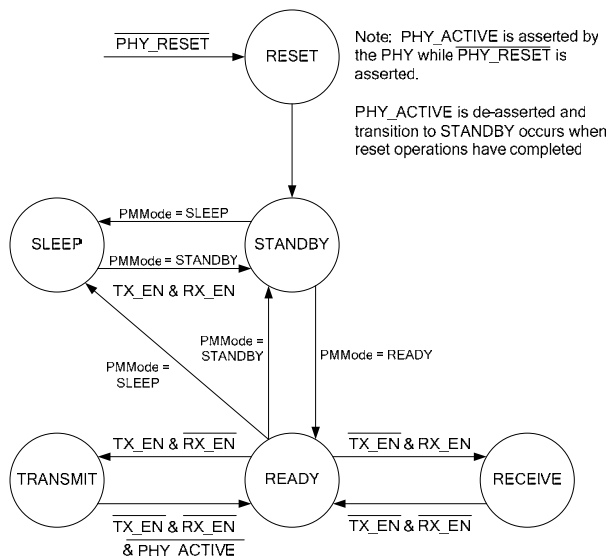


Figure 7-1 PHY State Transition Diagram

#### 7.1.1 PHY RESET PROTOCOL

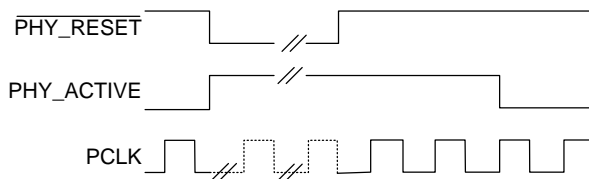


Figure 7-2 PHY Reset Protocol

At any time and from any PHY state including after initial power on, the MAC may force the PHY into RESET state by asserting control signal !PHY\_RESET. The PHY indicates entry to RESET state by asserting PHY\_ACTIVE and optionally stopping PCLK. Transitions on both !PHY\_RESET and PHY\_ACTIVE in this case are asynchronous to PCLK.

During reset, the PHY drives CCA\_STATUS, DATA\_EN and DATA[7:0] to their inactive values. The MAC drives RX\_EN, TX\_EN and SERIAL\_DATA to their inactive values. PHY\_ACTIVE is driven as described above.

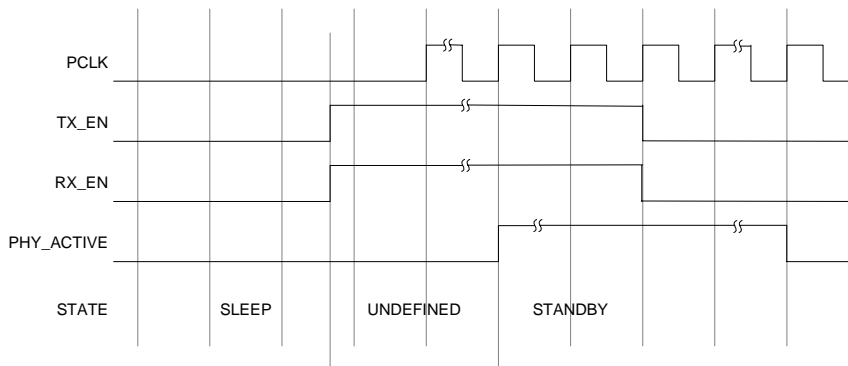
The MAC maintains !PHY\_RESET asserted for at least PHY specific interval PHYResetTime. After !PHY\_RESET is de-asserted the PHY completes its reset operations. When PCLK is stable (according to PHY specific conditions) the PHY de-asserts PHY\_ACTIVE to indicate transition to STANDBY state. The PHY is responsible for setting PMMODE to STANDBY and RDY to the appropriate value. If RDY is set by the PHY to indicate abnormal completion of RESET operation, the meaning of all registers except RDY is undefined.

#### 7.1.2 EXIT FROM SLEEP STATE

The MAC may place the PHY into SLEEP state by writing SLEEP to the PMMODE register (see Table 5-2). During SLEEP state, the PHY reduces power consumption by turning unnecessary functions off. However, the contents of the Dynamic Registers are maintained



through SLEEP and can be assumed unchanged after the PHY is returned to STANDBY state.



*Figure 7-3 Exit SLEEP protocol*

Exit from SLEEP state is carried out by the following operations :

- The MAC asserts both TX\_EN and RX\_EN
- When the PHY has reached STANDBY state, it asserts PHY\_ACTIVE and sets PMMODE to STANDBY
- When the MAC detects the rising edge of PHY\_ACTIVE, it de-asserts TX\_EN and RX\_EN
- The PHY responds by de-asserting PHY\_ACTIVE.

### 7.1.3 NORMAL OPERATION

By writing to the PHY configuration register PMMODE (see Section 5), the MAC controls transitions between any two of the three PHY states: SLEEP, STANDBY and READY except for transitions from SLEEP state which requires a special operation as described in section 7.1.2.

When the PHY is not actively transmitting or receiving, it will normally be in STANDBY state. In preparation for an active time period, the MAC must first put the PHY in READY state by writing into configuration register PMMODE. The MAC must put the PHY in READY state at least TurnOnDelay microseconds before commanding the PHY into TRANSMIT or RECEIVE state. After this delay, TRANSMIT or RECEIVE state can be initiated by the MAC asserting TX\_EN or RX\_EN respectively. The PHY is returned to READY state by de-asserting the same signal. (For complete transition conditions, see Transmit and Receive subsections later in this chapter.) Once the PHY is back in READY state, the MAC may either initiate another frame transmission or reception by again asserting TX\_EN or RX\_EN, or it may command the PHY back into STANDBY by writing to register PMMODE.

Table 7-1 gives the complete conditions for the PHY state transitions.

*Table 7-1 State Transition Conditions*

TRANSITION	TX_EN	RX_EN	WRITE TO PMMODE
RESET → STANDBY	LOW	LOW	—
STANDBY → SLEEP	LOW	LOW	SLEEP
SLEEP → STANDBY	HIGH	HIGH	—
STANDBY → READY	LOW	LOW	READY
READY → SLEEP	LOW	LOW	SLEEP
READY → STANDBY	LOW	LOW	STANDBY
READY → TRANSMIT	Rising edge	LOW	—
TRANSMIT → READY	Falling edge	LOW	—
READY → RECEIVE	LOW	Rising edge	—
RECEIVE → READY	LOW	Falling edge	—

## 7.2 FRAME TIMING

Precise frame timing is provided by the MAC (except when in Burst Mode as described in 7.7.3) for transmit operations and by the PHY/MAC for receive operations.

- Start of transmitted frame timing is indicated by the rising edge of TX\_EN associated with the PHY-dependent, but fixed, PHY transmit processing delay TxDelay for single frame transmission and for the 1st frame of a Burst transmission
- End of transmit frame timing is indicated by the falling edge of PHY\_ACTIVE
- Start of receive frame timing is indicated by the rising edge of PHY\_ACTIVE associated with the PHY-dependent, but fixed, PHY receive processing delay SyncDelay
- End of receive frame timing is indicated by the falling edge of PHY\_ACTIVE associated with the PHY-dependent, but fixed, PHY receive delay PhyActiveDelay.

## 7.3 RANGING SUPPORT

Ranging estimation may be optionally supported by the PHY. Capabilities are indicated by static parameter RangingSupported. If ranging is supported, timing of transmission and reception events may be controlled via the RNGEN bit [2] in the CONTROL [00h] dynamic parameter register.

PHYs which support ranging must provide up to a 32-bit ranging counter and indicate the precision of the timestamp by reference to the frequency of the ranging counter.

RNGEN is to indicate whether the PHY should set the RANGINGTIMER register from the ranging counter during transmission and reception.

The interface events associated with these timestamps are :

- The start of transmission of the preamble at the local antenna as indicated by the assertion of PHY\_ACTIVE
- The acquisition of the preamble as indicated by the assertion of PHY\_ACTIVE during reception.

These transitions on PHY\_ACTIVE provide support for ranging procedures which may be implemented within or above the MAC by indicating when ranging timestamps should be retrieved. However, the ranging timestamp value is not tied to the PCLK timing associated with PHY\_ACTIVE transitions. See Referenced Documents [5] for a definition of the ranging timestamp reference and Referenced Documents [6] for the associated calibration parameters RANGING\_TRANSMIT\_DELAY and RANGING\_RECEIVE\_DELAY.

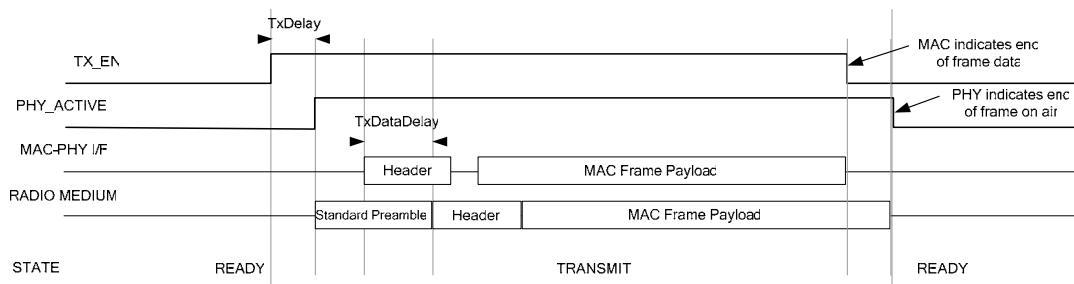
The processing of the timestamps by the MAC or higher layer functions is outside the scope of this specification. The Two-Way Time Transfer range measurement mechanism defined in Referenced Documents [2] uses the following MAC-PHY interface registers and parameters:

- RANGINGTIMER;
- RangingSupported,
- RANGING\_TRANSMIT\_DELAY,
- RANGING\_RECEIVE\_DELAY;
- PHYClockAccuracy.

Calculations are described in Referenced Documents [7].

## 7.4 TRANSCEIVER DELAY DEFINITIONS

Figure 7-4 and Figure 7-5 show the principle transceiver delay intervals for Transmit and Receive cases respectively.



*Figure 7-4 Transmit Delay Intervals*

TxDelay is the interval between the assertion of TX\_EN and the start of the first symbol of the preamble being present at the local antenna.

The PHY requests header data by asserting DATA\_EN no earlier than TxDataDelay before the end of the preamble as shown in Figure 7-4. TxDataDelay is measured backwards from the end of the preamble to provide a fixed, preamble independent, header processing interval for PHY implementations and a fixed interval between TX\_EN assertion and the first assertion of DATA\_EN to be used by the MAC for end of previous frame processing.

The MAC must drive valid data to DATA[7:0] 2 PCLK periods after DATA\_EN is asserted.

The PHY de-asserts PHY\_ACTIVE on the rising edge of the PCLK following the transmission of the end of the last symbol of the frame at the local antenna.

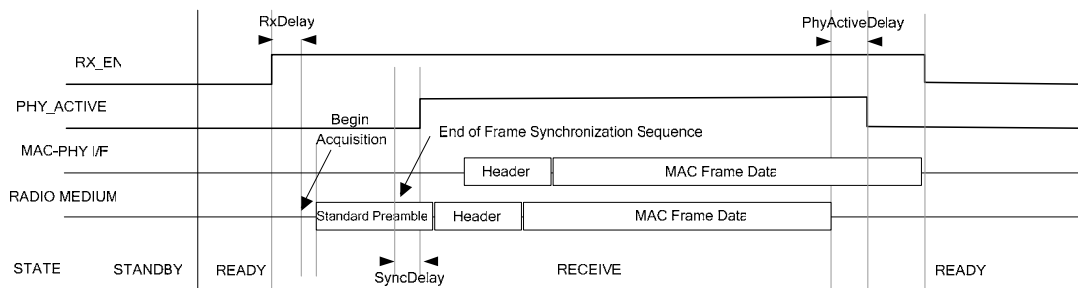


Figure 7-5 Receive Delay Intervals

RxDelay is the interval between the assertion of RX\_EN and the start of the preamble acquisition operation by the PHY.

Precise start of frame timing is provided by the PHY via the assertion of PHY\_ACTIVE a PHY-dependent but fixed delay, SyncDelay, after the end of last symbol of the preamble Frame Synchronization Sequence (preceding the Channel Estimation Sequence) arrives at the local antenna.

End of frame timing is provided by de-assertion of PHY\_ACTIVE a PHY-dependent, but fixed, delay, PHYActiveDelay, after the end of the last symbol is received at the local antenna. PHYActiveDelay compensates for the processing delay inherent in the PHY receive processing path.

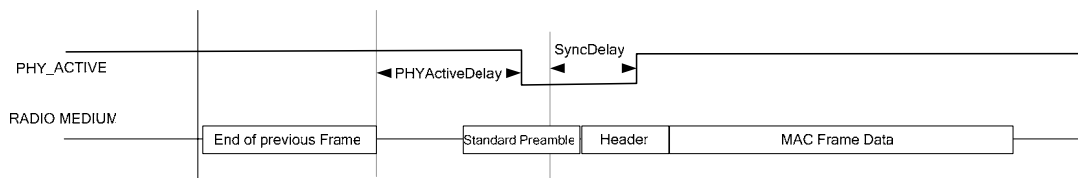


Figure 7-6 PHYActiveDelay Timing

As shown in Figure 7-6, PHYActiveDelay may overlap with the start of the preamble of the next receive frame but must permit PHY\_ACTIVE to be de-asserted before the end of the Frame Synchronization sequence to permit acquisition of the incoming frame to be signalled. It is the responsibility of the PHY vendor to specify the value of PHYActiveDelay such that this condition can be met for a zero length frame.

Precise end of frame timing can also be calculated from the known precise start of frame timing, preamble, PHY Header and MAC Frame Data structures, data rates and symbol encoding.

## 7.5 TRANSCEIVER TURNAROUND TIMES

### 7.5.1 RX-TX TURNAROUND TIME

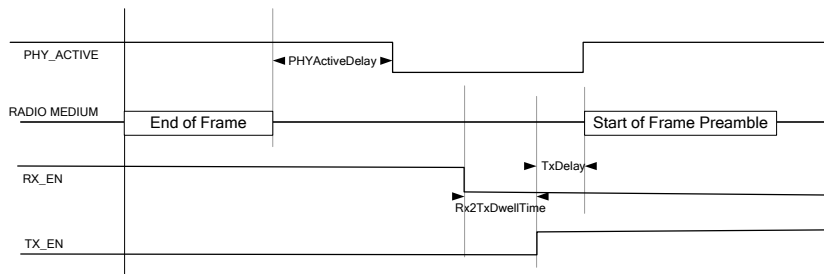


Figure 7-7 Rx-Tx Turnaround Time

The minimum interval between RX\_EN de-assertion and TX\_EN assertion shall be a fixed, PHY specific value, Rx2TxDwellTime. The following inequality shall be respected:

$$\text{PHYActiveDelay} + \text{Rx2TxDwellTime} + \text{TxDelay} < \text{SIFS}$$

## 7.5.2 TX-RX TURNAROUND TIME

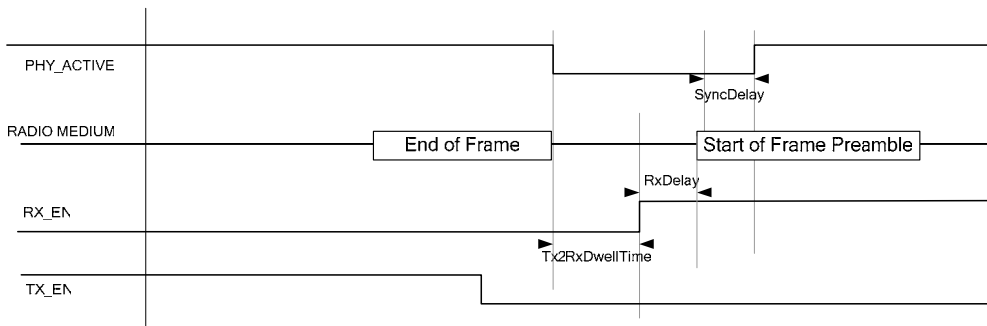


Figure 7-8 Tx-Rx Turnaround Time

The minimum interval between PHY\_ACTIVE de-assertion (in TRANSMIT State) and RX\_EN assertion shall be a fixed, PHY specific value, Tx2RxDwellTime. The following inequality shall be respected:

$$\text{Tx2RxDwellTime} + \text{RxDelay} < \text{SIFS}$$

## 7.6 PREAMBLE CONTROL

### 7.6.1 SINGLE FRAME TRANSMISSION AND RECEPTION

In each single frame transmission the Standard Preamble is transmitted.

- BM shall be set to '0' for single frame transmission
- PT shall be set to '0' for single frame transmission

In single frame reception, the preamble to be acquired by the receiver is defined by register RXPT which must be set, respecting the receive setup and hold times defined in 5.7.2, to indicate the Standard Preamble.

### 7.6.2 BURST MODE TRANSMISSION

A burst is defined as a MIFS separated sequence of frames (see 7.7.3). In burst transmission, the PHY assures the accurate MIFS timing between frames. The preamble to be transmitted with each frame is defined by the rules summarized below :

- BM shall be set to 1 for Burst Mode frame transmission.

#### 7.6.2.1 DATA RATES OF 200MBPS OR LOWER

For DATA RATES of 200Mbps or lower, all frames in the burst shall use the Standard Preamble.

- PT shall be set to '0' for data rates of 200Mbps or lower

#### 7.6.2.2 DATA RATES ABOVE 200MBPS

For DATA RATES above 200Mbps, the first frame in the burst shall use the Standard Preamble. The second and subsequent frames of the burst may use the Burst Preamble or the Standard Preamble.

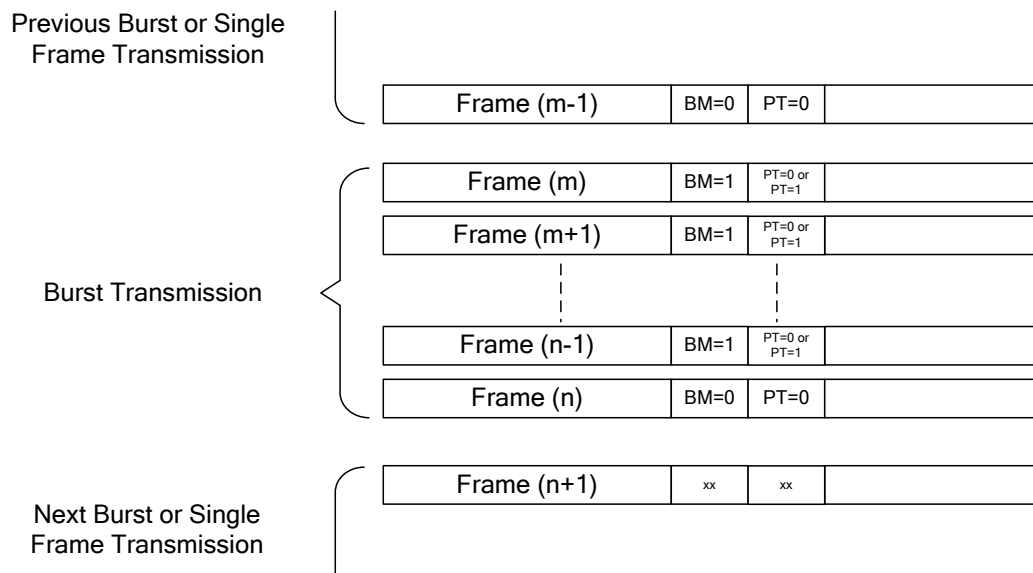


Figure 7-9 Burst transmission preamble control

As shown in Figure 7-9 a burst transmission begins with a frame (m) carrying BM = '1' in the PLCP Header, normally preceded by a frame (m-1) with BM = '0' and PT = '0'.

- The 1st frame in the burst (frame m) is transmitted with the Standard Preamble.
- The 2nd and subsequent frames (m+1,..., n) of the burst are transmitted with a preamble type defined by PT in the preceding (m,..., n-1) frame PLCP Header.
- The last frame (n) in the burst is transmitted with BM = '0' and PT = '0'.

### 7.6.3 BURST MODE RECEPTION

In burst mode reception the MAC maintains RX\_EN asserted between frames within the burst.

During burst mode reception, processing of PT when BM = '1' is performed automatically by the PHY when register PTON is set to '1'.

The MAC is responsible for all receive preamble control via register RXPT when register PTON is set to '0'.

A burst mode reception is terminated following reception of a frame with BM = '0' or immediately after RX\_EN is de-asserted.

## 7.7 TRANSMIT OPERATION

There are two transmit operations – Single Frame transmit and Burst Mode transmit.

In single frame transmission, a single frame is transferred from the MAC to the PHY and on-air timing is controlled by the state of TX\_EN and the PHY transmission of symbols at the local antenna. There is no specific operation following completion of the single frame transmission. The next operation could be another transmission, a receive or a transition to STANDBY.

In Burst Mode Transmit there is an explicit relationship between each frame in a sequence of frames. On-air timing is controlled by TX\_EN for the start of the first frame only. Subsequent frame timing is maintained by the PHY during the burst.

### 7.7.1 DATA BUS OWNERSHIP

The DATA[7:0] bus is driven by the MAC in TRANSMIT state. The MAC takes control of DATA[7:0] three clocks following TX\_EN assertion. The MAC relinquishes control two clocks after TX\_EN de-assertion regardless of the PHY requesting data by asserting DATA\_EN.

### 7.7.2 SINGLE FRAME TRANSMISSION CONTROL

The MAC has complete control over the single frame transmission operation. For each frame transmitted, the MAC sets the PLCP Header parameters listed in Table 7-2 in the Tx Frame format as defined in Figure 6-1.

The MAC also sets the Transmit control registers listed in Table 7-3 respecting the setup and hold times defined in Figure 5-4.

*Table 7-2 Single Frame Transmit Parameters*

PARAMETER	VALUE	COMMENT
SCRAMBLER	$  (S1..S2) + 1  _4$	S1 & S2 are treated as a 2-bit unsigned integer and incremented for each frame sent from the MAC to the PHY
BM	0	Burst Mode is always 0 for single frame transmissions
PT	0	Preamble Type is always 0 for single frame transmission
TX_TFC	T1..T3	TFC code used to transmit the frame
BG	BG lsb	Least-significant bit of Band Group
RATE	00000 .... 00111	Encoding of data rate for the MAC Frame Payload part of the frame. Value shall be set to 00000 if LENGTH is zero.
LENGTH	0...4095	Number of Octets in MAC Frame Payload part of Frame

*Table 7-3 Transmit Control Registers for Single Frame Transmit*

REGISTER	VALUE	COMMENT
TXCHAN	Valid Channel (see Referenced Documents [3])	Channel on which to perform the transmit operation
TXCTL-TXPT	0	The preamble is always the Standard Preamble in single frame transmissions
TXCTL-TXANT	0.. SupportedDiversity[5:4]	Identifies the transmit antenna
TXCTL-TXPWR	0.. NumTxPwrLevels-1	Transmit power level index
CONTROL- RNGEN	0 1	If RangingSupported = 0 RNGEN is set to 0 If RangingSupported = 1 RNGEN is set to 0 to disable RANGINGTIMER setting RNGEN is set to 1 to enable RANGINGTIMER setting

Figure 7-10 illustrates the transmission of a single frame, starting from READY state. The MAC starts the transmission by asserting TX\_EN while keeping RX\_EN low. When the PHY detects the rising edge of TX\_EN it transitions to TRANSMIT state, turns on the radio transmit path and begins to transmit the preamble defined by TXPT using its antenna defined by TXANT on the channel defined by TXCHAN.

The timing of TX\_EN assertion should be TxDelay ahead of nominal frame timing at the local antenna to compensate for PHY transmit processing delay.

In TRANSMIT State the PHY has full control over data flow. Data is requested from the MAC by asserting DATA\_EN at the rising edge of PCLK. The MAC must drive DATA[7:0] 2 clock cycles later.

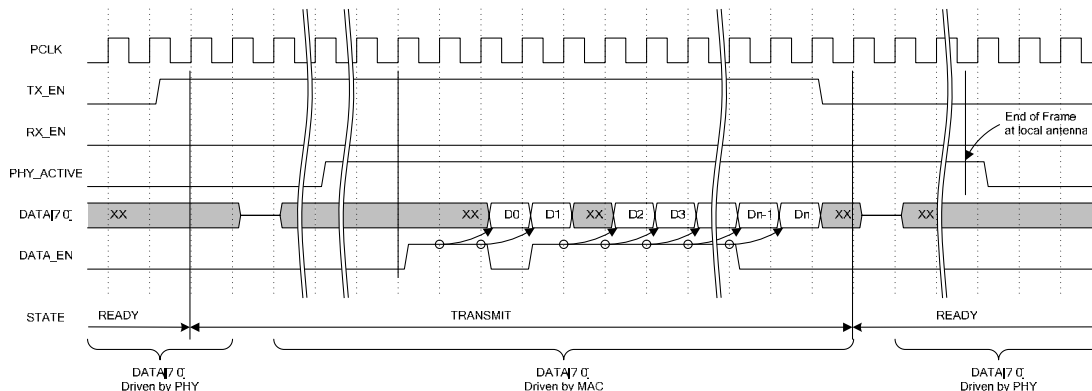


Figure 7-10 Single Frame Transmit Timing

The PHY performs the following operations :

- Asserts PHY\_ACTIVE at the rising edge of PCLK following the transmission of the leading edge of the first symbol of the preamble at the local antenna
- If RNGEN = 1 sets Dynamic Register RANGINGTIMER at the Ranging Reference Signal (defined in Referenced Documents [5] as the first sample of the first Channel Estimation Sequence of the preamble) according to the precision defined by the RangingSupported static parameter (see Table 5-1)
- Requests Header and Payload data (as appropriate) from the MAC by asserting DATA\_EN while respecting TxDataDelay.

The MAC performs the following operations :

- Transfers one octet of header or payload data (as appropriate) for each request from the PHY via a rising edge of DATA\_EN
- Completes the transmit operation by de-asserting TX\_EN at the rising edge of the PCLK cycle after the last octet of the frame FCS (or MAC Header if LENGTH is zero) has been transferred to the PHY

The PHY completes the single frame transmit operation by :

- De-asserting PHY\_ACTIVE at the rising edge of PCLK following the transmission of the trailing edge of the last symbol from the local antenna
- Transitioning back to READY state

This procedure is repeated for each transmitted frame. The MAC is responsible for calculating the start of frame timing in all cases.



A frame transmission can be aborted by the MAC at any time by de-asserting TX\_EN before the last octet of the FCS (or MAC Header if LENGTH is zero) has been transferred to the PHY (see 7.9).

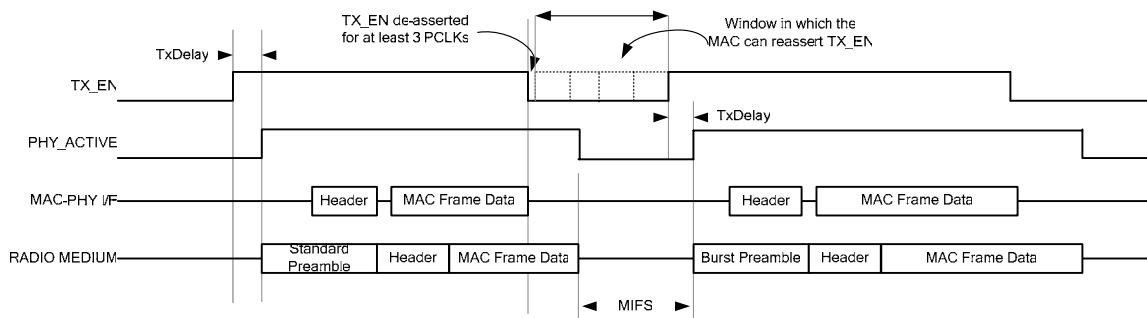
### 7.7.3 BURST MODE TRANSMISSION CONTROL

A burst is a sequence of MIFS separated frames transmitted from the same source. In burst mode transmission, the MAC has control over the timing of the first frame in the sequence of burst mode frames. The first frame is transmitted in exactly the same manner as a single frame transmission, as described in 7.7.2, except for the PLCP Header parameters listed in Table 7-4.

*Table 7-4 Unique Burst Mode PLCP Header parameters*

PARAMETER	VALUE	COMMENT
BM	1	Burst Mode must be set to 1 in the first frame of the burst mode sequence
PT	0	PT = 0 if the next frame will be sent using the Standard Preamble
	1	PT = 1 if the next frame will be sent using the Burst Preamble
LENGTH	1...4095	Number of Octets in MAC Frame Payload part of Frame

Timing for the transmission of subsequent frames in the burst is maintained by the PHY provided that TX\_EN is re-asserted within the window shown in Figure 7-11. The minimum duration TX\_EN shall remain de-asserted before re-assertion is three PCLK cycles.



*Figure 7-11 Burst Mode Transmission*

If the MAC re-asserts TX\_EN in this window, the PHY assures the start of the first symbol of the preamble of the next frame is presented at the local antenna exactly MIFS after the end of the last symbol of the previous frame. The MIFS interval is defined to be an exact number of symbols to enable the receiver to maintain synchronization from the Burst Preamble.

In burst transmission, the value of PT overrides TXPT in determination of which preamble the PHY transmits ahead of each PLCP header and MAC frame body (if present).

Each subsequent frame in the burst mode sequence is transmitted as in the single frame case except for the PLCP Header parameters in Table 7-4 and the assurance of the MIFS interval provided TX\_EN is re-asserted within the window defined in Figure 7-11, until the last frame in the sequence which differs in the PLCP parameters define in Table 7-5.

*Table 7-5 Unique Final Frame PLCP parameters*

PARAMETER	VALUE	COMMENT
BM	0	Burst Mode must be set to 0 in the last frame of the burst mode sequence
PT	0	PT must be set to 0 in the last frame of the burst mode sequence
RATE	00000 ... 00111	Encoding of data rate for the MAC Frame Payload part of the frame. Value shall be set to 00000 if LENGTH is zero.
LENGTH	0 ... 4095	Number of Octets in MAC Frame Payload part of Frame. Note the special case of a frame with LENGTH of zero is permitted since the MIFS interval will not be used following this frame.

#### 7.7.4 BURST MODE TRANSMIT ERROR RECOVERY

If TX\_EN is re-asserted:

- later than TxDelay before MIFS, but earlier than MIFS, after the end of the previous frame, the behaviour of the PHY is undefined
- later than MIFS after the end of the previous frame, the PHY shall abort burst mode transmission and return to normal transmission. The next assertion of TX\_EN will be treated as a single frame transmission or the first frame of a new burst mode transmission.

### 7.8 RECEIVE OPERATION

#### 7.8.1 DATA BUS OWNERSHIP

The DATA[7:0] bus is driven by the PHY in RECEIVE state. Valid data is indicated by the rising edge of DATA\_EN being asserted at the rising edge of PCLK.

#### 7.8.2 SINGLE FRAME RECEPTION CONTROL

The MAC has control over frame reception operations via the RX\_EN control signal. For each frame received, the MAC sets the Receive control registers listed in Table 7-6 respecting the setup and hold times defined in Figure 5-5. The PHY reports the received PLCP Header parameters in the receive frame format as describe in Figure 6-1.

Table 7-6 Receive Control Registers for Single Frame Receive

REGISTER	VALUE	COMMENT
RXCHAN	Valid channel (see Referenced Documents [3])	Channel on which to perform the receive operation
RXCTL-RXPT	0	RXPT is set to 0 if the PHY should seek to acquire a Standard Preamble. Single frames are always transmitted using the Standard Preamble.
RXCTL-RXANT	0.. SupportedDiversity[1:0]	Identifies the receive antenna
RXCTL-PTON	0 1	PTON is ignored for single frame reception
CONTROL-RNGEN	0 1	If RangingSupported = 0 RNGEN is set to 0  If RangingSupported = 1  RNGEN is set to 0 to disable RANGINGTIMER setting  RNGEN is set to 1 to enable RANGINGTIMER setting

The reception of a single frame is depicted in Figure 7-12, starting from the READY state. The MAC commands the PHY into RECEIVE state by asserting RX\_EN while keeping TX\_EN de-asserted.

When the PHY detects the rising edge of RX\_EN, it transitions to RECEIVE state, turns on the radio receive path, waits RxDelay and then starts a preamble acquisition as defined by RXPT using its receive antenna defined in RXANT on the channel defined in RXCHAN. RxDelay is the turn-on time for the radio receive path.

The PHY has full control over data flow during frame reception.

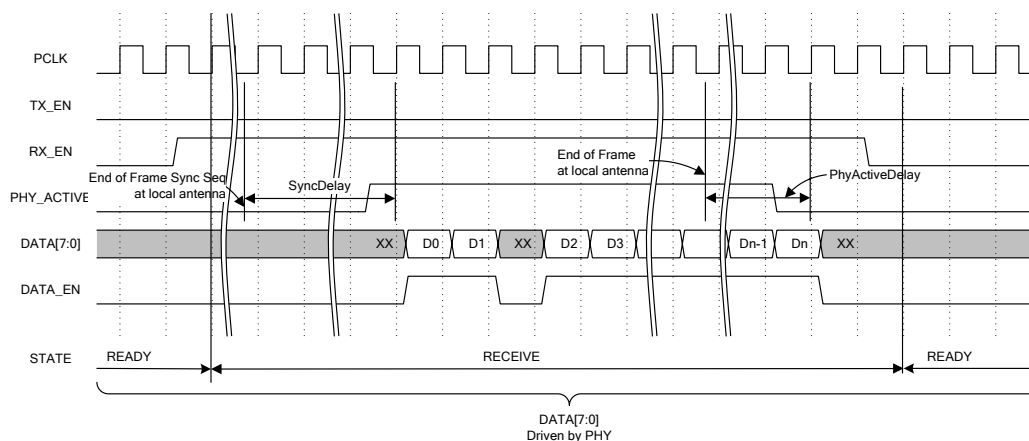


Figure 7-12 Single Frame Receive Timing Diagram

The PHY performs the following operations:

- The PHY will seek to acquire the specified preamble on the specified antenna and channel RxDelay after the assertion of RX\_EN

- Preamble acquisition is signaled by the PHY asserting PHY\_ACTIVE, as indicated in Figure 7-12. The delay between the end of the last symbol of the Frame Synchronization Sequence of the preamble (before the Channel Estimation Sequence) in the antenna and the raising edge of PHY\_ACTIVE is a PHY-dependent but fixed delay SyncDelay
- If RNGEN = 1 sets Dynamic Register RANGINGTIMER at the Ranging Reference Signal (defined in Referenced Documents [5]) according to the precision defined by the RangingSupported static parameter (see Table 5-1)
- The PHY decodes the received symbols and transfers the PLCP Header to the MAC by the assertion of DATA\_EN. At each PCLK rising edge with DATA\_EN asserted the MAC reads one octet of data into the RX Frame
- The PHY interprets the PLCP header parameters and computes the header checksum and compares it with the HCS field in the received PLCP header. The PHY reports the status of the header in HEADER\_ERROR as defined in Figure 6-1

The MAC performs the following operations on the RX Frame fields:

- Interprets the HEADER\_ERROR parameter. If any bit in HEADER\_ERROR is set, the MAC should perform frame recovery by de-asserting and re-asserting RX\_EN not less than 3 PCLK cycles later
  - If header checksum verification failed, the receive operation is terminated according to 7.11.2.1
  - If the PLCP header RATE is not supported, the PHY terminates the receive operation according to 7.11.2.2
- Interprets RX Frame field LENGTH – the length in octets of the MAC Frame Payload. The MAC uses this parameter as needed to support the transfer of received data from the DATA[7:0] bus

The MAC continues the receive operation, if HEADER\_ERROR reports no errors, transferring one octet of data for each rising edge of PCLK while DATA\_EN is asserted. After LENGTH octets have been received the MAC transfers the 4 octets of the FCS and 3 octets of receive quality information into the receive frame and processes the remaining parameters:

- RX Frame field FCS. The MAC computes the FCS according to its specified CRC algorithm and compares the result with the RX Frame FCS value to determine the validity of the MAC Frame Payload data
- RX Frame field RSSI – received signal strength indication. The MAC uses this value as required to support links with the transmitting device
- RX Frame field LQI – link quality indicator. The MAC uses this value as required to support links with the transmitting device
- RX Frame field RXERROR – receive error status. The MAC interprets any set bit in RXERROR as required to perform frame reception error handling

If the PHY had detected an unrecoverable payload error, the receive operation would have been terminated according to 7.11.2.3.

The PHY completes the receive operation by :

- De-asserting PHY\_ACTIVE at the rising edge of PCLK a PHY-dependent but fixed delay, PHYActiveDelay, after the trailing edge of the packet waveform at the local antenna

The MAC completes the receive operation by :

- De-asserting RX\_EN. The PHY remains in RECEIVE state until RX\_EN is de-asserted by the MAC, at which point it transitions back to READY.

A frame reception can be aborted before completion by de-asserting RX\_EN as described in section 7.10.

### 7.8.3 BURST MODE RECEPTION CONTROL

In Burst Mode reception the receiving MAC commands the PHY to perform continuous frame reception by maintaining RX\_EN asserted following reception of a frame with BM set to 1. Each frame received with BM = 1 is processed in a manner identical to single frame reception except for the de-assertion of RX\_EN to complete the reception operation. The frame symbol timing is determined by the transmitter but the receiving PHY can exploit the PLCP header BM and PT fields to improve receive performance.

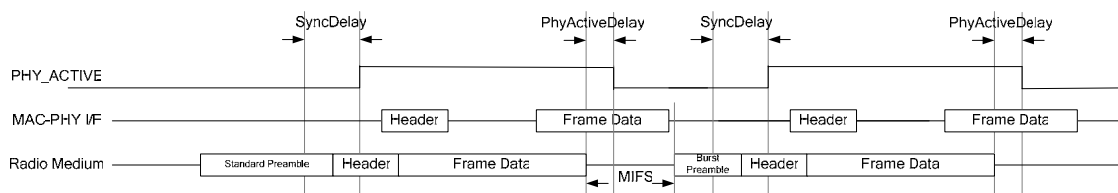
There is one receive control register specific to burst mode as shown in Table 7-7.

*Table 7-7 Unique Burst Mode Receive Registers*

PARAMETER	VALUE	COMMENT
RXCTL-PTON	0	When PTON = 0, the MAC must control all receive preamble acquisition via RXPT
	1	When PTON = 1, the PHY interprets the PT field in PLCP headers with BM = 1

Following reception of a frame with BM = 1 and PT = p, the PHY will prepare to receive a new preamble exactly MIFS after the end of that frame using the preamble indicated by RXPT if PTON = 0, or the preamble indicated by p if PTON = 1.

Figure 7-13 shows a sequence of burst mode received frames with MIFS separation. The timing of each frame is bracketed by the assertion and de-assertion of PHY\_ACTIVE with SyncDelay and PhyActiveDelay as in the case of single frame reception.



*Figure 7-13 Burst Mode Receive with MIFS*

As long as each received frame carries BM = 1 the MAC maintains RX\_EN asserted and the PHY will continue to perform acquisition and frame reception, each time using the preamble as defined by the previously received PT value or the RXPT value depending on the setting of PTON.

The burst is terminated upon receipt of a frame with BM = 0 after which the MAC de-asserts RX\_EN in an identical manner to that for single frame reception.

### 7.8.4 BURST MODE RECEPTION ERROR RECOVERY

At any time within a burst, the MAC may recover from reception errors and terminate Burst Mode reception by de-asserting RX\_EN.

### 7.8.5 ZERO LENGTH FRAME RECEPTION

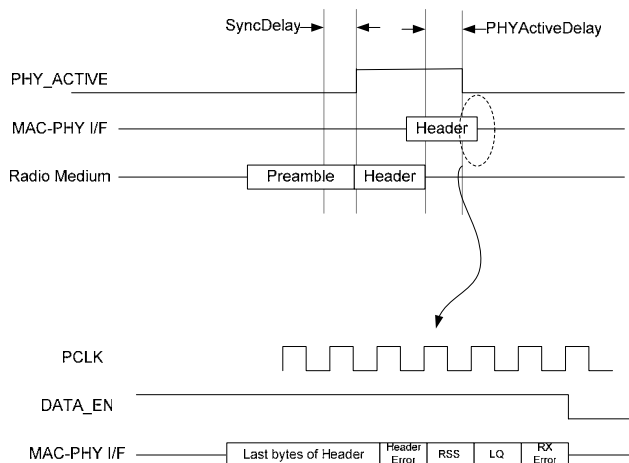


Figure 7-14 Zero Length Frame Reception

Figure 7-14 shows zero length frame reception and presentation of the associated receive parameter block (RSSI, LQI and RXERROR) following the HEADER\_ERROR octet.

The receive parameters do not necessarily follow immediately after the HEADER\_ERROR octet as the PHY may exploit flow control via DATA\_EN when delivering the receive parameter block.

Note that DATA\_EN is always used to qualify DATA[7:0] as the PHY retains full flow control during receive operation.

### 7.9 MAC TRANSMIT ABORT

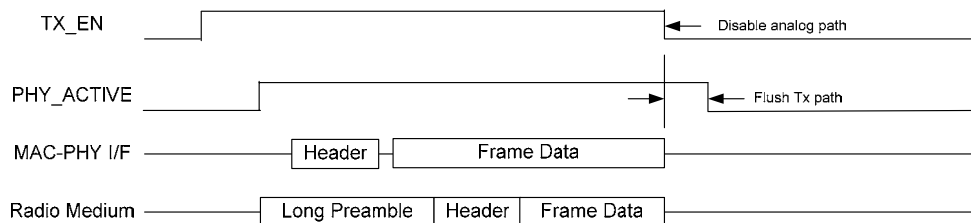


Figure 7-15 MAC Aborted Transmit

Figure 7-15 shows the operation of the interface when the MAC de-asserts TX\_EN before delivering the last octet of the FCS to the DATA[7:0] bus.

Upon detecting de-assertion of TX\_EN, the PHY should immediately disable the path to the local antenna so that no further symbols are transmitted but may take the necessary time to flush the transmit logic before de-asserting PHY\_ACTIVE at the rising edge of PCLK and returning to READY state.

Note that it is assumed that immediate cessation of transmission at the local antenna is expected to require disabling the analog transmit path. The PHY will normally require additional time to reset the digital transmission path before being ready to resume normal operation.

## 7.10 MAC RECEIVE ABORT

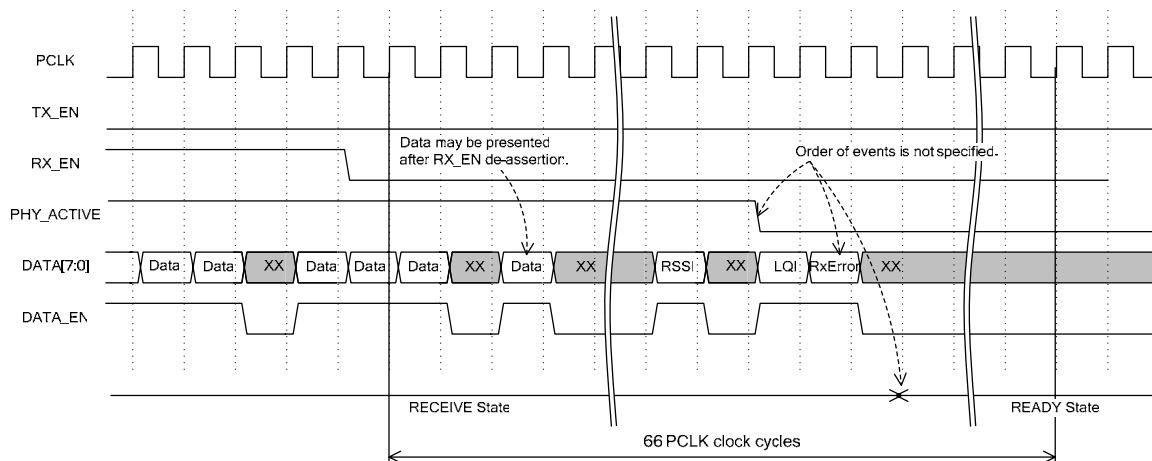


Figure 7-16 MAC Aborted Receive Timing Diagram

Figure 7-16 shows the operation of the interface when the MAC de-asserts RX\_EN before the end of frame has been received at the local antenna. Normal RECEIVE operation requires that RX\_EN be asserted until after the last octet of the receive parameter block (RXERROR) has been presented to the MAC at the DATA[7:0] bus and validated by DATA\_EN.

- The MAC may abort a receive operation at any time after asserting RX\_EN by de-asserting RX\_EN

If RX\_EN is de-asserted at any time before this last octet transfer, irrespective of whether PHY\_ACTIVE is asserted or de-asserted, the following abort operation occurs:

- Within 66 PCLK clock cycles of detecting the de-assertion of RX\_EN, the PHY shall abort the receive operation, shall stop transferring data to the MAC, shall present the receive parameter block which will be qualified by DATA\_EN and shall de-assert PHY\_ACTIVE (if asserted)
- If 19 or more octets of data, including the PHY header, the MAC header and HEADER\_ERROR have been delivered by the PHY, the MAC shall consider the last three octets delivered by the PHY within these 66 PCLK clock cycles to be the receive parameter block
- Otherwise, all data delivered by the PHY for the aborted receive operation is undefined.

The order in which PHY\_ACTIVE is de-asserted and the receive parameter block is presented is not specified but must complete within 66 PCLK cycles after de-assertion of RX\_EN.

(A special case should be noted for Burst Mode - if the acquisition of the next frame is signaled by the assertion of PHY\_ACTIVE before the completion of delivery of the data and receive quality block of the preceding frame, de-assertion of RX\_EN will abort both the delivery of the preceding frame and the incoming frame.)

## 7.11 ERROR CONDITIONS

### 7.11.1 TRANSMIT ERROR CONDITIONS

There are no defined error conditions that occur during transmit operations.

### 7.11.2 RECEIVE ERROR CONDITIONS

#### 7.11.2.1 HEADER CHECKSUM ERROR

The PHY computes the header checksum (HCS) for the received PHY Header and compares it with the value in the header HCS field. If this check fails, the contents of the

header cannot be trusted – including the critical LENGTH parameter that defines the extent of the MAC Frame Payload field.

In this case, the PHY sets the HEADER\_ERROR bits in the receive frame data structure. The PHY then behaves as if a zero length frame had been received.

Even though the header checksum fails to validate the header, the Rx Frame will contain the following:

- The PLCP header including the RATE and LENGTH
- The MAC header
- The HEADER\_ERROR bits
- RSSI
- LQI
- RXERROR

The PHY shall de-assert PHY\_ACTIVE at a suitable interval after detection of the header checksum failure. In this HCS error case, end of frame timing derived from the de-assertion of PHY\_ACTIVE is not valid. HEADER CHECKSUM ERROR is set in both HEADER\_ERROR and RXERROR fields.

If the MAC maintains RX\_EN asserted following the indication of HCS error, the PHY will continue to seek to acquire a frame using the same preamble type used in the frame whose header checksum failed.

If the Preamble type needs to be re-set (e.g. after failure to acquire a Burst Preamble, the MAC may set the preamble to Standard Preamble) the MAC should de-assert RX\_EN, set RXPT to the appropriate value and re-start the PHY's acquisition operation by re-asserting RX\_EN. It is the MAC's responsibility to determine the timing of re-acquisition following a lost frame, including loss of an intermediate frame in a burst.

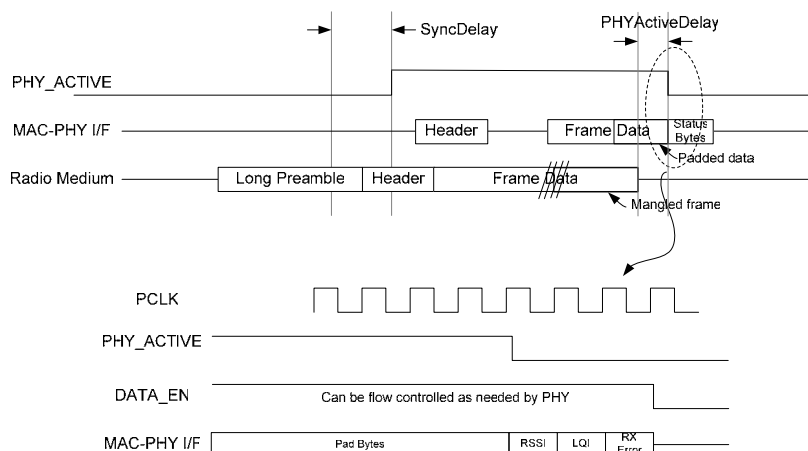
#### **7.11.2.2 UNSUPPORTED DATA RATE**

If the data values in the PHY and MAC Header are validated by the HCS but one or more of the parameters is set to an unsupported value (e.g. Rate), the PHY sets the HEADER\_ERROR bits in the receive frame data structure and performs a zero length frame receive operation as described in 7.11.2.1.

The PHY shall de-assert PHY\_ACTIVE at a suitable interval after detection of the unsupported data rate. The corresponding error bits are set in both the HEADER\_ERROR and RXERROR fields.



### 7.11.2.3 UNRECOVERABLE DETECTED PAYLOAD ERROR



*Figure 7-17 Unrecoverable Payload Error Handling*

Figure 7-17 shows how an incoming frame aborted by the PHY is signaled after the PHY detects an unrecoverable error while receiving the frame body.

In this case, the PHY can use the content of the PLCP header which has been received with a good HCS. The PHY uses the LENGTH field to determine how many octets of the frame body remain to be transferred to the MAC via the DATA[7:0] bus.

The PHY pads this many undefined value octets at DATA[7:0], qualified by DATA\_EN to complete the receive frame operation. PHY\_ACTIVE is de-asserted at the nominal end of frame at the local antenna that the PHY computes from LENGTH plus PHYActiveDelay (see Figure 7-17). The receive quality block is transferred as for a normally completed receive operation.

The PHY sets the PAYLOAD\_ERROR bit in RXERROR to signal the aborted receive. In addition, the undefined value pad octets will in general cause the MAC FCS check to fail.

## 7.12 CLEAR CHANNEL ASSESSMENT

The CCA Interface is used for Clear Channel Assessment status indication. It consists of the CCA\_STATUS signal and the following dynamic registers:

*Table 7-8 CCA Dynamic Registers*

ADDRESS	REGISTER	BIT	FIELD	R/W	DESCRIPTION	INIT.
00(h)	CONTROL	3	CCRE	R/W	The MAC controls CCA estimation by the PHY by writing to CCRE.  0 Stop CCA Estimation 1 Start CCA Estimation	0

Other Dynamic Registers may be provided in the Vendor Specific Register area for enhanced control of the CCA operation since measurement intervals and detection thresholds are highly dependent on the design of the estimation circuit.

### 7.12.1 CCA INTERFACE SIGNALS

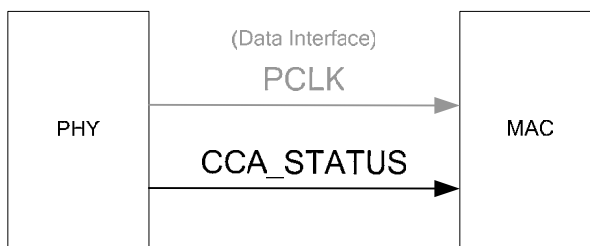


Figure 7-18 CCA Interface Signals

Table 7-9 CCA Interface Signals

SIGNAL NAME	WIDTH	DIRECTION	FUNCTION
CCA_STATUS	1	PHY-MAC	CCA status. 0 indicates that the wireless medium is idle. 1 indicates that the medium is busy.

### 7.12.2 OPERATION OF THE CCA INTERFACE

The MAC writes a '1' to the CCRE field of the CONTROL register, using the Management Interface, to initiate a CCA measurement.

CCA\_STATUS will be driven after PHY specific but constant interval CCAValidTime according to the implementation dependent CCA estimation algorithm, and will be valid as long as the PHY is not in TRANSMIT, STANDBY or SLEEP state. Estimation will continue as long as CCRE is set to '1'.

The MAC writes a '0' to CCRE, using the Management Interface, when CCA estimation is no longer required.

All other CCA operations will depend on vendor specific register settings.

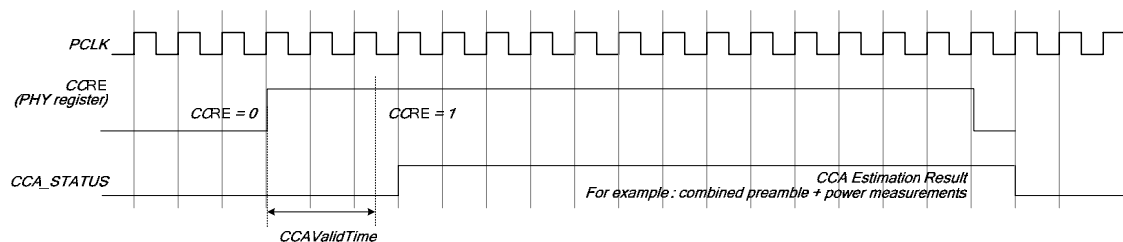


Figure 7-19 CCA Operating Timing Diagram

7.13 MANAGEMENT INTERFACE

7.13.1 MANAGEMENT INTERFACE SIGNALS

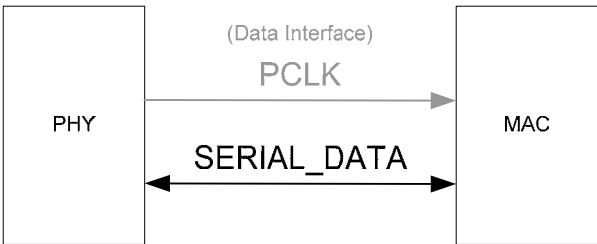


Figure 7-20 Management Interface Signals

Table 7-10 Management Interface Signal Definitions

SIGNAL	DIRECTION	DESCRIPTION
SERIAL_DATA	MAC to PHY	For write operations, the MAC drives register address and register data to the PHY
	PHY to MAC	For read operation, the MAC drives register address to the PHY. The PHY drives register data to the MAC
Note. It is the responsibility of the MAC to ensure the SERIAL_DATA signal is driven to the ‘0’ level except during READ or WRITE operations.		

7.13.2 OPERATION OF THE MANAGEMENT INTERFACE

7.13.2.1 READ OPERATION

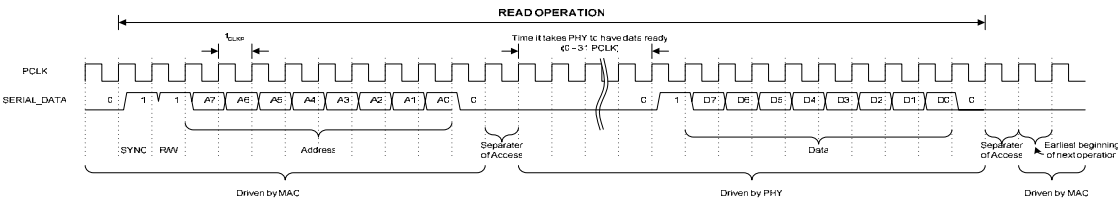


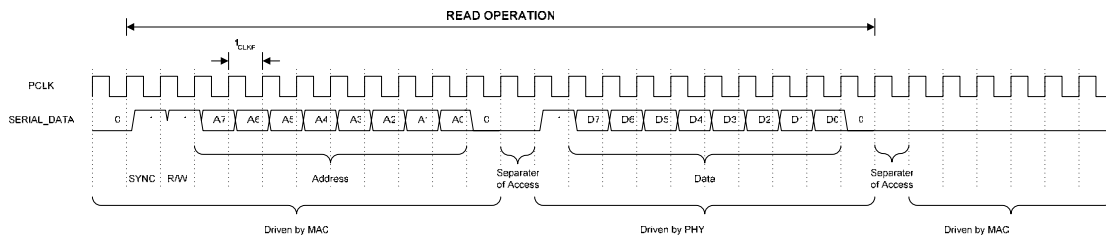
Figure 7-21 Serial Read Operation

For a serial read operation, the MAC drives the first part of the transaction, which includes the PHY register address. The PHY drives the second part of the transaction, which includes the requested data. Regardless of whether the MAC or PHY drives the Management Interface, every bit driven on the SERIAL\_DATA line is always synchronized with PCLK.

The MAC will drive a “1” as the first bit on the SERIAL\_DATA pin. The second bit is a “1”, which indicates a read operation. The MAC drives the next 8 bits, which are the PHY register address. This allows the MAC to address up to 256 PHY configuration registers. After the 8-bit address, the MAC drives a ‘0’ bit to place the SERIAL\_DATA line in a known state.

The PHY drives ‘0’ to the SERIAL\_DATA line for a period from 0 to 31 PCLK cycles beginning on the second PCLK after the MAC stops driving the interface.

The PHY drives a ‘1’ bit to indicate start of data followed by 8 data bits. The transaction is completed by driving a terminating ‘0’ bit to place the SERIAL\_DATA line in a known state before releasing the line to be driven by the MAC.

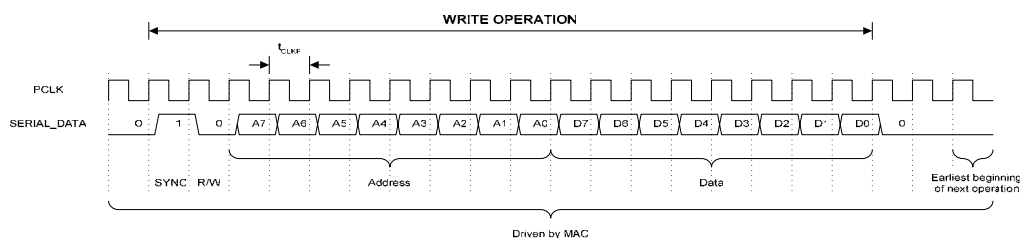


*Figure 7-22 Fastest Read Response*

Figure 7-22 shows the timing for the fastest PHY response to a read operation.

(Note: Implementer can use internal or external pull-down resistors to set the SERIAL\_DATA pin to 0 when the MAC is no longer driving the signal.) The MAC will resume control of the SERIAL\_DATA pin.

### 7.13.2.2 WRITE OPERATION

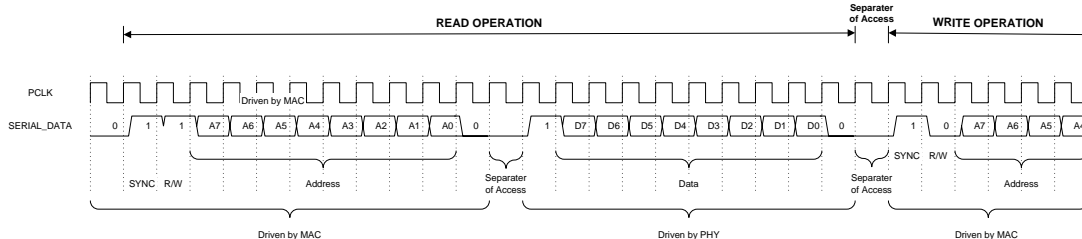


*Figure 7-23 Serial Write Operation*

For a serial write operation, the MAC drives the entire transaction. Each bit the MAC drives on the SERIAL\_DATA pin is synchronized with PCLK.

The MAC will drive a “1” as the first bit on the SERIAL\_DATA pin. The second bit is a “0”, which indicates a write operation. The next 8 bits are the PHY address location. This allows the MAC to address up to 256 octets of PHY configuration registers. The next 8 bits are the data to be written to the addressed PHY register. At the end of 8 bits of data, the MAC will drive a terminating “0.” Once the transaction is complete the MAC stops driving the management interface.

(Note: Implementer can use internal or external pull-down resistors to set the SERIAL\_DATA pin to 0 when the MAC is no longer driving the signal.) The SERIAL\_DATA pin will continue to be controlled by the MAC.



*Figure 7-24 Read Operation Followed By Write Operation*

Figure 7-24 shows the fastest timing for a read operation followed immediately by a write operation.

### 7.13.3 EXAMPLES

#### 7.13.3.1 READ OPERATION EXAMPLE

The MAC wants to read the PHYID (addresses 0x20h and 0x21h). PHYID is 1B86 hex stored in big-endian representation. In this example it takes the PHY four clock cycles to have the data available.

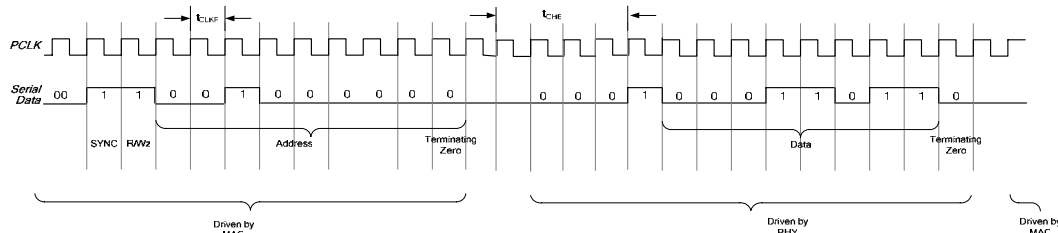


Figure 7-25 Serial Read Example, Address 20hex

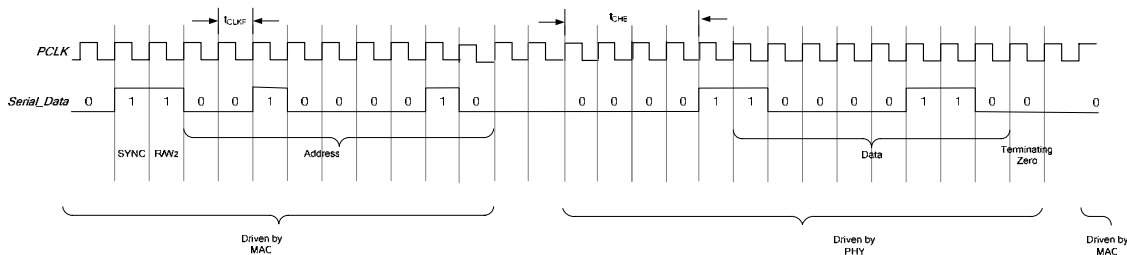


Figure 7-26 Serial Read Example, Address 21hex

#### 7.13.3.2 WRITE OPERATION EXAMPLE

MAC wants to put PHY into READY state by setting PMMODE=0. (PMMODE address is 06, READY State is value 0.)

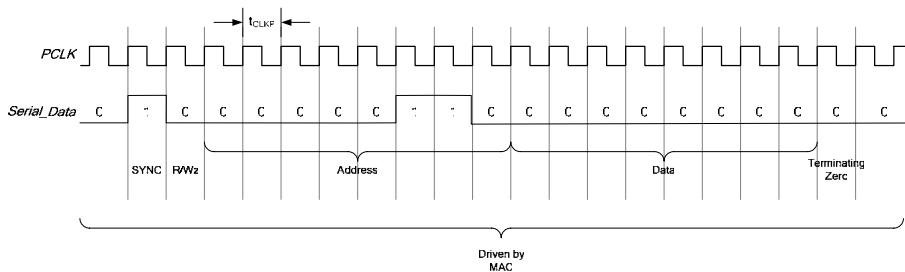


Figure 7-27 Serial Write Example Address 06 hex

## Appendix A ELECTRICAL SPECIFICATIONS

### A.1 I/O DC REQUIREMENTS

To improve interoperability between MACs and PHYs from different vendors the following voltage parameters are recommended:

#### A.1.1 3.3V DC SPECIFICATION

Appendix Table A-1 gives the Operating Range under nominal parameter values:

- $V_{CC} = 3.0V$  to  $3.6V$
- Ambient Temperature =  $0^{\circ}C$  to  $70^{\circ}C$

*Appendix Table A-13.3V Functional Operating Range*

	PARAMETER	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS	NOTES
	$V_{CC}$	Supply Voltage		3.0	3.6	V	
INPUT	$V_{IH}$	Input high voltage		2	$V_{CC}+0.5$	V	1
	$V_{IL}$	Input low voltage		-0.3	0.8	V	1
	$I_{IL}$	Input leakage current	$0 < V_{in} < V_{CC}$	-10	+10	$\mu A$	2, 3
	$C_{IN}$	Input pin capacitance			10	pF	
OUTPUT	$V_{OH}$	Output high voltage	$I_{out} = -4mA$	2.4		V	2
	$V_{OL}$	Output low voltage	$I_{out} = 4mA$		0.4	V	2

### A.1.2 1.8V DC SPECIFICATION

Appendix Table A-2 gives the Operating Range under nominal parameter values:

- $V_{CC} = 1.65V$  to  $1.95V$
- Ambient Temperature =  $0^{\circ}C$  to  $70^{\circ}C$

*Appendix Table A-2 1.8V Functional Operating Range*

	PARAMETER	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS	NOTES
	$V_{CC}$	Supply Voltage		1.65	1.95	V	
INPUT	$V_{IH}$	Input high voltage		1.2	$V_{CC}+0.2$	V	1
	$V_{IL}$	Input low voltage		-0.2	0.7	V	1
	$I_{IL}$	Input leakage current	$0 < V_{in} < V_{CC}$	-600	+600	$\mu A$	2, 3
	$C_{IN}$	Input pin capacitance			2	pF	
OUTPUT	$V_{OH}$	Output high voltage	$I_{out} = -8mA$	$0.8* V_{CC}$	$V_{CC}$	V	2
	$V_{OL}$	Output low voltage	$I_{out} = 8mA$	0	$0.2* V_{CC}$	V	2

### A.1.3 1.2V DC SPECIFICATION

Appendix Table A-3 gives the Operating Range under nominal parameter values:

- $V_{CC} = 1.1V$  to  $1.3V$
- Ambient Temperature =  $0^{\circ}C$  to  $70^{\circ}C$

*Appendix Table A-3 1.2V Functional Operating Range*

	PARAMETER	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS	NOTES
	$V_{CC}$	Supply Voltage		1.1	1.3	V	
INPUT	$V_{IH}$	Input high voltage		0.8	$V_{CC} + 0.2$	V	1
	$V_{IL}$	Input low voltage		-0.2	0.4	V	1
	$I_{IL}$	Input leakage current	$0 < V_{in} < V_{CC}$	-120	+120	$\mu A$	2, 3
	$C_{IN}$	Input pin capacitance			2	pF	
OUTPUT	$V_{OH}$	Output high voltage	$I_{out} = -4mA$	$0.7* V_{CC}$	$V_{CC}$	V	2
	$V_{OL}$	Output low voltage	$I_{out} = 4mA$	0	$0.3* V_{CC}$	V	2

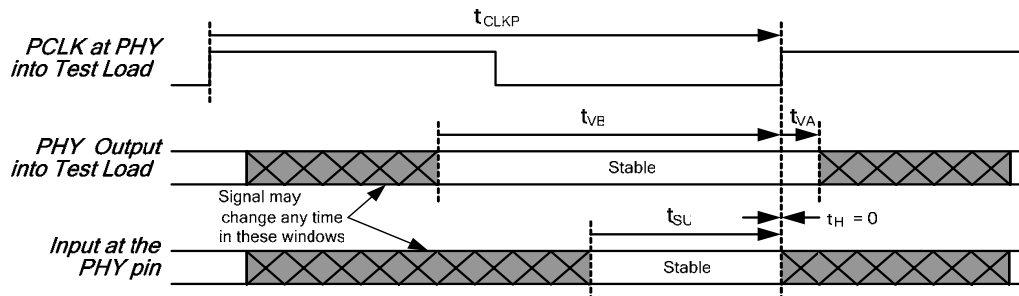
Notes:

1. This is a DC specification. During transitions the inputs may experience overshoot beyond  $V_{IH}(\max)$  and undershoot below  $V_{IL}(\min)$ .
2. Positive current is defined into the pin.
3. Input leakage currents include Hi-Z outputs leakage for bi-directional buffers with tri-state outputs.

## A.2 MAC PHY TIMING SPECIFICATIONS

### A.2.1 PHY SIGNAL TIMINGS

To improve interoperability between MACs and PHYs from different vendors the following timings for synchronous signals at the PHY are recommended:



Appendix Figure A-1 PHY Signal Timing Diagram

Appendix Figure A-1 shows the signal timings for the PHY. Both input and output timings are specified with respect to rising edge of PCLK driven into the specified test load of 10pF crossing  $V_{meas} = 1.4V$ .

Output timings are specified with the PHY pins driven into the specified test load of 10pF, and are measured at  $V_{meas} = 1.4V$ .

Input timings are specified at the PHY pin to  $V_{IL}(\max)$  for a logic 0 and  $V_{IH}(\min)$  for logic 1.

All transitions, except those on !PHY\_RESET and STOPC, are synchronous with the rising edge of PCLK.

Appendix Table A-4 defines the values for the PHY timing requirements.

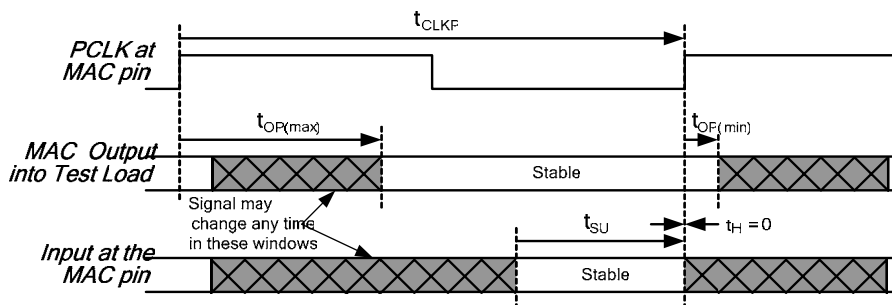
Appendix Table A-4 PHY Signal Timing Values

VALUE	DESCRIPTION	MAX	MIN
$t_{CLKP}$	PHY Clock Period	-	15nS
$t_{VB}$	Time PHY output data is valid before the rising edge of PCLK	-	9ns
$t_{VA}$	Time PHY output data is valid after the rising edge of PCLK	-	1ns
$t_{SU}$	Setup time, to rising edge of PCLK	-	5ns
$t_H$	Hold time, from rising edge of PCLK	-	0ns



### A.2.2 MAC SIGNAL TIMINGS

To improve interoperability between MACs and PHYs from different vendors the following timings for synchronous signals at the MAC are recommended:



*Appendix Figure A-2 MAC Signal Timing Diagram*

Appendix Figure A-2 shows the signal timings for the MAC. Both input and output timings are specified with respect to rising edge of PCLK at the MAC pin crossing  $V_{\text{meas}} = 1.4\text{V}$ .

Output timings are specified with the MAC pin driven into the specified test load of 10pF, and are measured at  $V_{\text{meas}} = 1.4\text{V}$ .

Input timings are specified at the MAC pin to  $V_{\text{IL}}(\text{max})$  for a logic 0 and  $V_{\text{IH}}(\text{min})$  for logic 1.

All transitions, except those on !PHY\_RESET and STOPC, are synchronous with the rising edge of PCLK.

Appendix Table A-5 defines the values for the MAC signal timing requirements.

*Appendix Table A-5 MAC Signal Timing Values*

VALUE	DESCRIPTION	MAX	MIN
$t_{\text{CLKP}}$	PHY Clock Period	-	15ns
$t_{\text{OP}}$	Time MAC output data is valid from the rising edge of PCLK	6ns	1ns
$t_{\text{SU}}$	Setup time, to rising edge of PCLK	-	5ns
$t_{\text{H}}$	Hold time, from rising edge of PCLK	-	0ns

## Appendix B PHY VENDOR AND VERSION CODING

The static parameters defined in 5.3 include two PHY identification parameters – PHYID and PHYVersion. The format and coding of these two variables is defined below. Management of the allocation of values to Vendor ID is under the control of the WiMedia Alliance Inc.

### B.1 PHYID FORMAT AND CODING

Appendix Figure B-1 shows the format of the PHYID parameter.

PHYID[15:8]	
Product Code (bits [15:11])	Product Version (bits [10:8])
PHYID[7:0]	
Vendor ID (bits [7:0])	

*Appendix Figure B-1 PHYID Format*

The first octet of PHYID contains the Vendor ID. The coding and values for vendor IDs are maintained by the WiMedia Alliance Inc.

The second octet of PHYID contains a 5-bit product code followed by a 3-bit product version number. The coding of product number and version are vendor defined.

### B.2 PHY VERSION FORMAT AND CODING

Appendix Figure B-2 shows the format of the PHYVersion parameter.

PHYVersion [7:0]	
Major Version Number (bits [7:4])	Minor Version Number (bits [3:0])

*Appendix Figure B-2 PHYVersion Format*

The PHYVersion parameter contains a 4-bit major version number and a 4-bit minor version number and declares the version of the WiMedia Multiband OFDM PHY specification to which the PHY implementation complies.

The version numbers are maintained by the WiMedia Alliance Inc.