MAC-PHY INTERFACE SPECIFICATION

Making High-Speed Wireless A Reality...

RELEASE 1.5

DECEMBER 1, 2009

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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1 Introduction

This document defines a functional interface between a WiMedia PHY implementation and a WiMedia MAC implementation.

Section 4 defines the interface signals and their functions.

Section 5 defines the interface parameters. A recommended mapping for PHY parameters is provided along with the register map for PHY registers and setup and hold timing for register access.

Section 6 defines the frame structure for data exchanges over the interface.

Section 7 provides the interface theory of operation. It covers PHY states and transitions, reset protocol, sleep protocol, frame timing references, preamble control, transmit and receive operations for single frames as well as burst mode operation, receive error cases, Clear Channel Assessment signal definition, and finally management interface and protocol.

Appendix A specifies electrical parameters of the interface. Appendix B defines formats for two WiMedia managed identifiers. Appendix C has notes concerning maintaining backward compatibility with Version 1.2.

1.1 Referenced Documents

[1] Multiband OFDM Physical Layer Specification, Version 1.5, March 26, 2009.

[2] Distributed Medium Access Control (MAC) for Wireless Networks, Version 1.5, December 1, 2009.

[3] WiMedia Assigned Numbers, Version 1.2.1, October 24, 2008.

2 Notational Conventions

The use of the word *shall* is meant to indicate a requirement which is mandated by the standard, i.e. it is required to implement that particular feature with no deviation in order to conform to the standard. The use of the word *should* is meant to recommend one particular course of action over several other possibilities, however without mentioning or excluding these others. The use of the word *may* is meant to indicate that a particular course of action is permitted. The use of the word *can* is synonymous with is able to – it is meant to indicate a capability or a possibility.

All floating-point values have been rounded to four decimal places.

3 Abbreviations and Acronyms

BM	Burst Mode
CC	Convolutional Code
CCA	Clear Channel Assessment
CRC	Cyclic Redundancy Code
ETSI	European Telecommunications Institute
FCC	Federal Communications Commission
FCS	Frame Check Sequence
FFI	Fixed-Frequency Interleaving
HCS	Header Check Sequence
LDPC	Low Density Parity Check
LQI	Link Quality Indicator

LSB	Least Significant Bit
MAC	Medium Access Control
MBOA	Multiband OFDM Alliance
MIFS	Minimum Inter-frame Space
MSB	Most Significant Bit
OFDM	Orthogonal Frequency Division Modulation
PHY	Physical (layer)
PLCP	Physical Layer Convergence Protocol
PPM	Parts per Million
PSMI	Parallel/Serial Management Interface
PT	Preamble Type
RSSI	Received Signal Strength Indicator
RX	Receive or Receiver
SIFS	Short Inter-frame Space
TF	Time-Frequency
TFC	Time-Frequency Code
TFI	Time-Frequency Interleaving
TX	Transmit or Transmitter
UWB	Ultra Wideband

4 Interface Signal Description

The MAC-PHY signal interface is depicted in Figure 4-1. It consists of the Data Interface including an 8-bit data bus, the Control Interface, the CCA Interface and the Management Interface. The Data Interface, which is used to transfer data to and from the MAC, operates differently depending on the state of the PHY. The Control Interface is used by the MAC to control the operating state of the PHY and by the PHY to indicate TX/RX status to the MAC. The CCA Interface is used for Clear Channel Assessment status indication. The Management Interface is used to access the PHY registers.

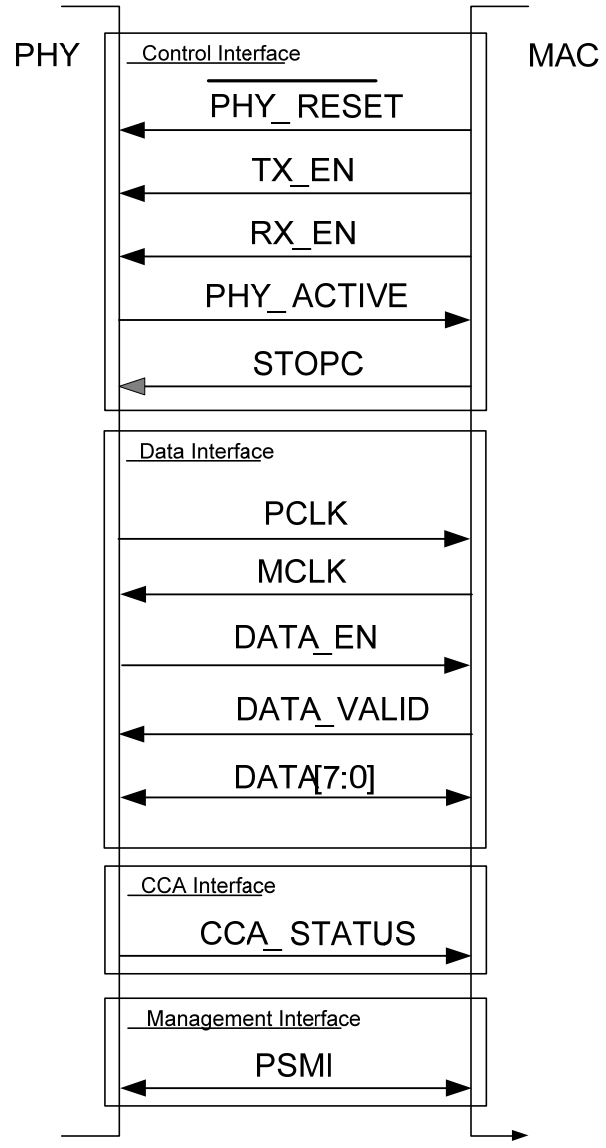


Figure 4-1 PHY-MAC Interface Signals

Table 4-1, Table 4-2, Table 4-3 and Table 4-4 define the signals in the Control Interface, Data Interface, CCA Interface and Management Interface, respectively. The operational mode of the Data Interface in each PHY state is summarized in Table 4-5.

4.1 Interface Signal Definitions

4.1.1 Control Interface

Table 4-1 Control Interface Signals

SIGNAL	WIDTH (BITS)	DIR	DESCRIPTION
!PHY_RESET	1	MAC to PHY	!PHY_RESET is asserted for PHY specific interval PHYResetTime to clear all PHY variables and reset the PHY to its initial state. The PHY writes STANDBY to PMMODE and transitions to STANDBY state after !PHY_RESET is de-asserted and reset operations have completed. !PHY_RESET is asynchronous to PCLK and MCLK. !PHY_RESET is ACTIVE LOW
TX_EN	1	MAC to PHY	TX_EN is used to place the PHY in TRANSMIT State. [Its secondary use (with RX_EN) is to transition from SLEEP to STANDBY when the PHY clock source has been stopped for power saving.] TX_EN is synchronous to MCLK, except in SLEEP state[1]. TX_EN is ACTIVE HIGH.
RX_EN	1	MAC to PHY	RX_EN is used to place the PHY in RECEIVE State. Its secondary use (with TX_EN) is to transition from SLEEP to STANDBY when the PHY clock source has been stopped for power saving. RX_EN is synchronous to MCLK, except in SLEEP state[1]. RX_EN is ACTIVE HIGH.
PHY_ACTIVE	1	PHY to MAC	PHY_ACTIVE is used by the PHY to indicate that it is either transmitting or receiving a frame over the air. In TRANSMIT state, the rising edge of PHY_ACTIVE indicates the start of frame at the local antenna and the falling edge indicates that the entire frame has been transmitted over the air. In RECEIVE state, the rising edge of this signal indicates preamble detection (with preamble starting precisely at SyncDelay plus the preceding synchronization fields before the PHY_ACTIVE rising edge), and the falling edge indicates the entire frame has been received at the local antenna (reception completed PHYActiveDelay before the PHY_ACTIVE falling edge). PHY_ACTIVE is also used in exit from SLEEP and RESET. PHY_ACTIVE is synchronous to PCLK. PHY_ACTIVE is ACTIVE HIGH.
STOPC (optional)	1	MAC to PHY	On/Off signal for PCLK in STANDBY state. PCLK is active when STOPC is de-asserted and not active when STOPC is asserted. STOPC is asynchronous to PCLK and MCLK. STOPC is ACTIVE HIGH.

(1) Although TX_EN and RX_EN are synchronous to MCLK, MCLK is not required to be enabled when these signals toggle.

4.1.2 Data Interface

Table 4-2 Data Interface Signals

SIGNAL	WIDTH (BITS)	DIR	DESCRIPTION
PCLK	1	PHY to MAC	Interface clock provided by the PHY. Interface signals originating from the PHY are synchronous to the rising edge of PCLK (see Appendix A). The nominal rate of PCLK is 66MHz.
MCLK	1	MAC to PHY	Interface clock provided by the MAC. Interface signals originating from the MAC are synchronous to the rising edge of MCLK (see Appendix A). MCLK is nominally a delayed version of PCLK.
DATA_EN	1	PHY to MAC	In TRANSMIT state this signal is used by the PHY to request more data from the MAC. In RECEIVE state, it is used to indicate to the MAC that there is valid data on the DATA[7:0] bus. DATA_EN is synchronous to PCLK. DATA_EN is ACTIVE HIGH.
DATA_VALID	1	MAC to PHY	In TRANSMIT state, this signal is used by the MAC to indicate data requested by the PHY is valid on the DATA[7:0] bus. DATA_VALID is synchronous to MCLK. DATA_VALID is ACTIVE HIGH.
DATA[7:0]	8	Bi-directional	DATA[7:0] is an 8-bit wide data bus driven by the MAC in TRANSMIT state and by the PHY in RECEIVE state. In all other states including SLEEP the bus driver is controlled by the mode of the Management Interface (see section 7.13.2 for detailed description). DATA[7:0] is synchronous to PCLK when driven by the PHY. DATA[7:0] is synchronous to MCLK when driven by the MAC. DATA[7:0] '1' is HIGH.

4.1.3 CCA Interface

Table 4-3 CCA Interface Signals

SIGNAL	WIDTH (BITS)	DIR	DESCRIPTION
CCA_STATUS	1	PHY to MAC	The PHY returns CCA_STATUS after a CCA request is initiated by the MAC writing to the CCRE register via SERIAL_DATA. CCA_STATUS is synchronous to PCLK. CCA_STATUS is ACTIVE HIGH.

4.1.4 Management Interface

Table 4-4 Management Interface Signals

SIGNAL	WIDTH (BITS)	DIR	DESCRIPTION
PSMI (Parallel/Serial Management Interface)	1	Bi-directional	The Management interface is used to access the control and configurations registers in the PHY. The PSMI signal has two modes of operation: Parallel mode and serial mode. The default mode is serial. If the PHY supports parallel mode operation (as defined in the MPI capabilities static register), the MAC can place the interface in parallel mode. In serial mode the MAC writes control and address bits to PSMI to initiate register access. The MAC then drives PSMI with data for Write operations serially. For read operations the PHY drives the PSMI signal with the Read data. In parallel mode the MAC writes control information on PSMI to initiate register access. The address and data are placed on the 8 bit DATA bus. For read operations the PSMI signal is driven by the PHY as an enable for the 8 bit data driven on the DATA bus. PSMI is synchronous to MCLK during the address phase and data WRITE operation. PSMI is synchronous to PCLK during the data READ operation. PSMI '1' is HIGH.

4.2 PHY Operational State

Table 4-5 PHY Readiness State

STATE	DESCRIPTION
RESET	Transitional state in which the configuration parameters are reset to default values. PCLK is undefined (see Section 7.1.1).
SLEEP	The radio is off. PCLK is off (see Section 7.1.2).
STANDBY	The radio is off. PCLK is on (unless STOPC is asserted). STANDBY is a higher activity state than SLEEP.
READY	Parts of the radio are on. PCLK is on.
TRANSMIT	The PHY Tx paths and the radio transmit path are active. PCLK is on.
RECEIVE	The PHY Rx paths and the radio receive path are active. PCLK is on.

5 Registers

Two sets of parameters are defined to allow the MAC to control the operation of the PHY and permit information to be provided by the PHY to the MAC.

- STATIC Parameters

  These parameters are fixed for a given instantiation of the MAC and PHY. They can be considered to be constants for the purposes of the definition of the MAC-PHY Interface and their values can be defined in a given PHY data sheet, stored as constants in the system implementation or provided by any other means. The static parameters are defined in Table 5-1.

- DYNAMIC Parameters

  These parameters may be changed during operation of the system, and affect operation of the PHY. They shall be implemented within the PHY as registers and can be read and/or written (depending on the specific parameter) via the Parallel/Serial Management Interface. The dynamic registers are defined in Table 5-2.

5.1 Bit Ordering and Interpretation

All data structures, except where explicitly stated, are defined with the bit order as shown in Figure 5-3.

Reserved bits shall be ignored on reading and set to ‘0’ on writing.

5.2 Register Address Space

The PHY has 256 addressable 8-bit registers (8-bit address, 8-bit data) divided into 3 regions:

1) Dynamic Register region defined by this specification : address 00(h)~1F(h)
2) Optional Static Parameter region defined by this specification : address 20(h)~7F(h)
3) Vendor Specific Register region for vender defined registers : address 80(h)~FF(h)

5.3 Static Parameters Definitions

Table 5-1 Description of Static Parameters

REGISTER	OCTETS	DEFINITION
SupportedRegDomains	2	Supported regulatory domains. Bit set to 1 if supported, and set to 0 otherwise. First Octet Bit Domain [2:0] Reserved [3] European Telecommunications Standards Institute (ETSI) [4] Federal Communication Commission (FCC) [5] Industry Canada (IC) [6] Association of Radio Industries and Business (ARIB) [7] Ministry of Information and Communication (MIC) (Korea) Second Octet Bit Domain [7:0] Reserved
SupportedDataRates	3	Set of supported data rates. Bit set 1 if supported, and set to 0 otherwise. Bit Data Rate Supported [0] 53.33 Mbps (CC) [1] RESERVED [2] 80 Mbps (CC) [3] 106.67 Mbps (CC) [4] RESERVED [5] 160 Mbps (CC) [6] 200 Mbps (CC) [7] 320 Mbps (CC) [8] 400 Mbps (CC) [9] 480 Mbps (CC) [10] 640 Mbps (LDPC) [11] 800 Mbps (LDPC) [12] 960 Mbps (LDPC) [13] 1024 Mbps (LDPC) [14] RESERVED [15] RESERVED [16] 160 Mbps (LDPC) [17] 200 Mbps (LDPC) [18] 320 Mbps (LDPC) [19] 400 Mbps (LDPC) [20] 480 Mbps (LDPC) [21] RESERVED [22] RESERVED [23] RESERVED
NumChannelsSupported	1	Number of supported channels

SupportedDiversity	1	Number of additional antennas provided for diversity [1:0] Number of receive antennas [3:2] Reserved [5:4] Number of transmit antennas [7:6] Reserved
SupportedChannels	1	Supported Channels. Bit set to 1if supported and set to 0 otherwise. Bit Channel Supported [0] TFC channels in band group 1 supported [1] TFC channels in band group 2 supported [2] TFC channels in band group 3 supported [3] TFC channels in band group 4 supported [4] TFC channels in band group 5 supported [5] TFC channels in band group 6 supported [7:6] RESERVED
TXPowerLevel	16	Array of transmit power levels. Array elements 0 to NumTxPowerLevels contain supported transmit power levels, in decreasing order of transmit power, i.e., element 0 corresponds to maximum transmit power level. Power level representation is vendor-specific. All other array elements shall be set to 0.
NumTxPowerLevels	1	Number of supported transmit power levels minus one. Acceptable range is zero to 15, with zero corresponding to supporting a single (fixed) transmit power level. [3:0] – Number of supported transmit power levels minus one [7:4] – RESERVED
SupportedPHYStates	1	Supported PHY States. Bit set to 1 if supported and set to 0 otherwise. [0] SLEEP [1] STANDBY [2] READY [3] TRANSMIT [4] RECEIVE [7:5] RESERVED
PHYClockAccuracy	1	Accuracy of PHY clock. Units ppm.
PHYResetTime	1	Interval during which !PHY_RESET shall be held asserted for the PHY to perform RESET operation. Units us.
WakeUpDelay	2	Time to transition from SLEEP mode to STANDBY mode. Units 0.5 us
TurnOnDelay	2	Radio turn-on time during transition from STANDBY mode to READY mode. Units 0.5 us.
TxDataDelay	1	Delay, not greater than 4us, before the end of the preamble at the local antenna before which the PHY will not assert DATA_EN to request the first octet of header data. See Section 7.4. Units us.
RxDataDelay	2	Maximum delay from the end of the received PLCP header at the local antenna to the transfer of the last octet of the PLCP header and HeaderError octet across the MAC-PHY interface. Units ns.
TxEOFDelay	2	Minimum delay from the transfer of the last octet of the frame across the MAC-PHY interface to the end of the frame at the local antenna. Units ns.

RxEOFDelay53.3	2	Maximum delay, at 53.3 Mbps, from the de-assertion of PHY_ACTIVE to the last de-assertion of DATA_EN corresponding to the transfer of the last octet of the frame and receive quality block across the MAC-PHY. Units PCLK cycles.
RxEOFDelayOther	2	Maximum delay, at all rates other than 53.3 Mbps, from the de-assertion of PHY_ACTIVE to the de-assertion of the last DATA_EN corresponding to the transfer of last octet of the frame and receive quality block across the MAC-PHY. Units PCLK cycles.
TxDelay	2	Delay from the rising edge of TX_EN to the time when the PHY feeds the leading edge of the preamble waveform to the antenna. Units ns.
RxDelay	2	Delay from the rising edge of RX_EN to the time when the PHY begins the preamble acquisition processing. Units ns.
Tx2RxDwellTime	2	Minimum interval between PHY_ACTIVE de-assertion (in TRANSMIT State) and RX_EN assertion. Units ns.
Rx2TxDwellTime	2	Minimum interval between RX_EN de-assertion and TX_EN assertion. Units ns.
SyncDelay	2	Delay from the end of the last symbol of the Frame Synchronization Sequence of the preamble waveform in the local antenna to the time when the PHY asserts PHY_ACTIVE. Note that since the preamble arrives asynchronously with respect to PCLK, PHY vendors should provide this value for the shortest amount of time before PHY_ACTIVE could be asserted assuming optimal alignment of the received preamble and PCLK. Units ns
TxSetupTime	2	Minimum time between setting of transmit control registers and assertion of TX_EN. Units PCLK cycles.
RxSetupTime	2	Minimum time between setting of receive control registers and the assertion of RX_EN or de-assertion of PHY_ACTIVE. Units PCLK cycles.
TxHoldTime	2	Minimum time between the assertion of TX_EN and changing transmit control registers for the next frame. Units PCLK cycles.
RxHoldTime	2	Minimum time between the assertion of RX_EN or deassertion of PHY_ACTIVE, and changing receive control registers for the next frame. Units PCLK cycles.
PHYID	2	PHY identifier to specify vendor, product and version. See Appendix B for format and coding.
PHYVersion	1	Version number of WiMedia PHY specification supported. See Appendix B for format and coding.

PHYActiveDelay	2	Delay from the end of the last symbol of the frame received in the local antenna and PHY_ACTIVE de-assertion. Note that since received frames arrive asynchronously with respect to PCLK, PHY vendors should provide this value for the shortest amount of time before PHY_ACTIVE could be de-asserted assuming optimal alignment of the received frame and PCLK. Units ns
CCAValidTime	1	The interval following the MAC setting CCRE to 1, after which the PHY should respond with CCA measurement result. Units 0.5μs.
MinPTChangeLength	1	Minimum MAC Frame Payload length for the preamble type of the next frame to be different to the current frame. Fixed value = 1 octet.
RangingSupported	1	Support for ranging; each bit below is set to 1 if the corresponding feature is supported, and set to 0 otherwise. [0] General ranging support [1] 528MHz counter (56.8 cm precision) (mandatory if ranging is supported) [2] 1056MHz counter (28.4 cm precision) (optional) [3] 2112MHz counter (14.2 cm precision) (optional) [4] 4224MHz counter (7.1cm precision) (optional) [5] Support for RANGINGTIMER [23:16] [6] Support for RANGINGTIMER [31:24] [7] RESERVED
RANGING_TRANSMIT_DELAY	2	The time from the generation of the reference signal (which triggers a ranging timer capture in PHY) to the time the signal reaches the device antenna. See the ranging section in Reference [1] for details. Units 4224 MHz clock periods.
RANGING_RECEIVE_DELAY	2	The time from the arrival of the reference signal at the antenna to the time the signal is first detected in the PHY (which triggers a ranging timer capture in PHY). See the ranging section in Reference [1] for details. Units 4224 MHz clock periods.
STOPC_OFF	1	Number of PCLK cycles from de-assertion of STOPC to PCLK stable. Units PCLK cycles.
ToneNullingSupported	1	Level of support for Tone Nulling information [0] Set to 1 if tone nulling is supported, and set to 0 otherwise. [7:1] RESERVED
MPI Capabilities	1	[0] Set to 1 if MCLK input is supported [1] Set to 1 if PHY is DDR capable [2] Set to 1 if PHY is Parallel Management Interface capable [7:3] RESERVED
PCLK Speed	1	[7:0] Number of clock cycles per microsecond. Nominal value at power-up is 66.

5.4 Static Parameter Coding

If the values of the static parameters are stored in the PHY, they should be implemented as read only values using the addresses and formats shown in Figure 5-1and Figure 5-2.

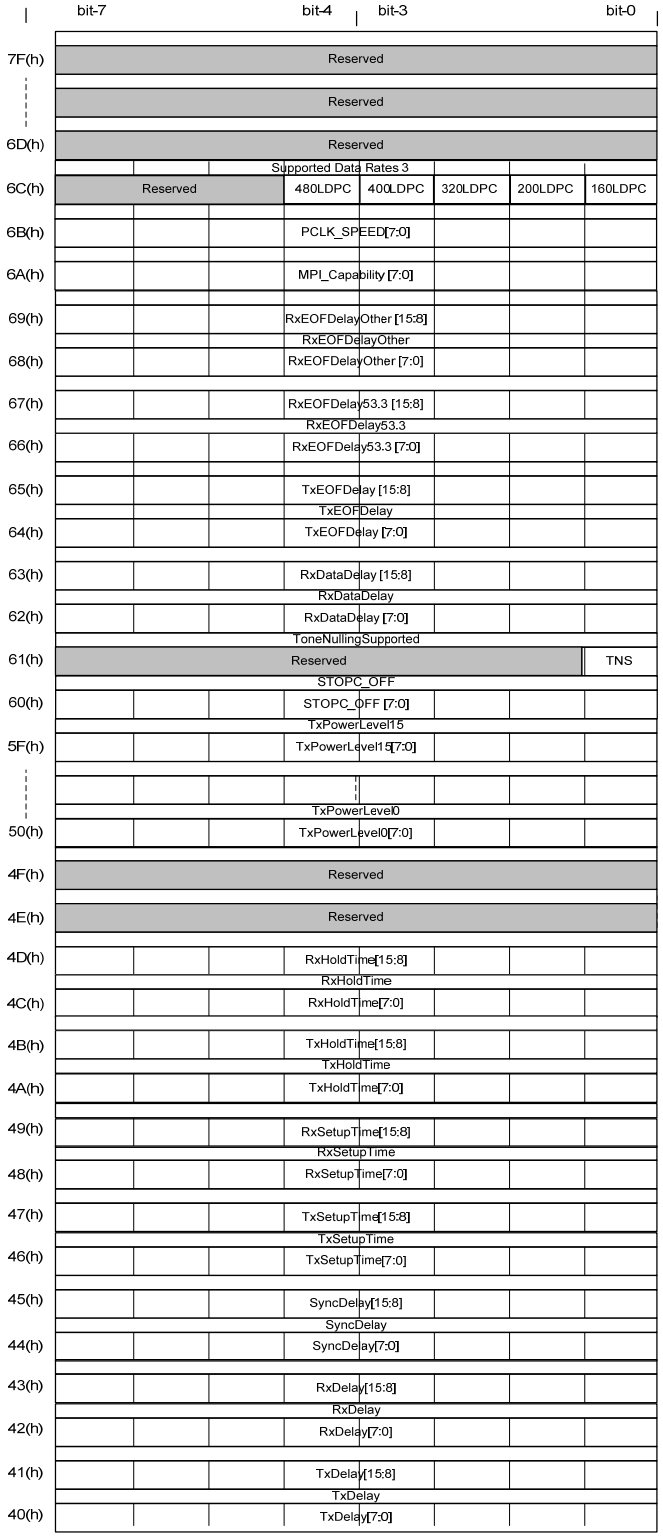


Figure 5-1 Static Parameter Encoding 40(h) - 7F(h)

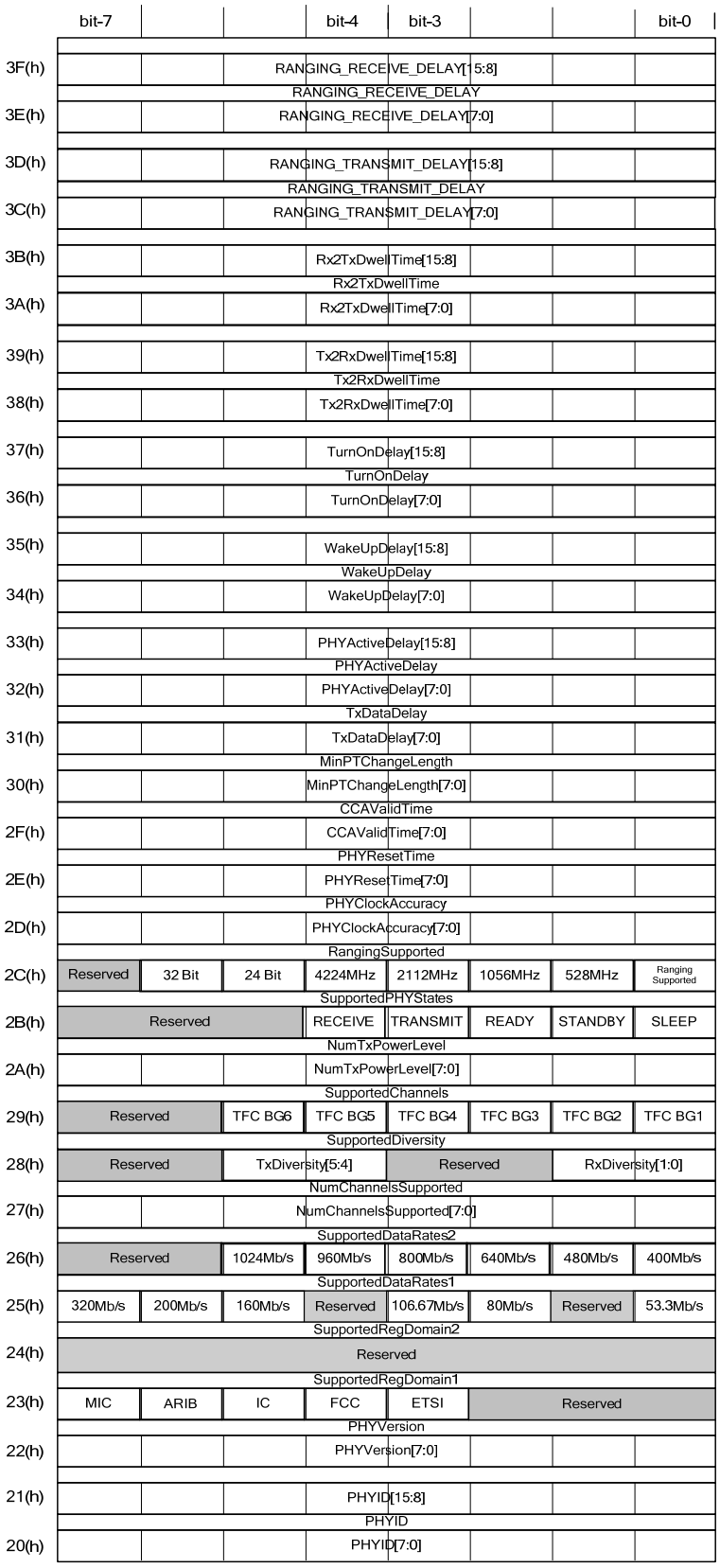


Figure 5-2 Static Parameter Encoding 20(h) - 3F(h)

5.5 Dynamic Registers Definitions

All registers in the Dynamic Register area are readable (R) and writable (W) by the MAC except RDY in the CONTROL register and RANGINGTIMER which are Read Only.

It is intended that the Current Regulatory Domain (CRD) register is not writable by a user application and can only be set by initialization or reset operations to ensure compatibility with regional regulatory requirements.

Table 5-2 Description of Dynamic Registers

ADDR.	REGISTER	R/W	DESCRIPTION	INIT.
00(h)	CONTROL	R/W (except RDY, which is R	PHY Control register [0] RDY - Result of reset operation. 0 = Normal completion of initialization 1 = Abnormal completion of initialization [1] Reserved [2] RNGEN 0 = RANGINGTIMER not set by PHY 1 = RANGINGTIMER set by PHY [3] CCRE – CCA Request 0 = Stop CCA estimation 1 = Start CCA estimation [7:4] RESERVED	0(h)
01(h)	CRD	R/W	[2:0] RESERVED [7:3] Current Regulatory Domain (CRD); each domain is mapped to a bit in the register, as follows, Bit Domain 3 European Telecommunications Standards Institute (ETSI). 4 Federal Communication Commission (FCC). 5 Industry Canada (IC). 6 Association of Radio Industries and Business (ARIB). 7 Association Ministry of Information and Communication (MIC) (Korea)	0(h)
02(h)	TXCHAN	R/W	TXCH - Channel of next transmitted frame [2:0] TFC [2:0] - least significant 3 bits of TFC [5:3] BG[2:0] – Band Group [6] TFC[3] – most significant bit of TFC [7] RESERVED Note: TXCH is coded as a 3-bit Band Group and a 4-bit TFC as defined in Reference [1].	0(h)

03(h)	TXCTL	R/W	Transmit Control [0] TXPT – Preamble type of next transmitted frame. 0 = Standard Preamble 1 = Burst Preamble [1] Reserved [3:2] TXANT – Transmit antenna to be used. Value 0..SupportedDiversity[5:4] where: 00 identifies transmit antenna 1 01 identifies transmit antenna 2 10 identifies transmit antenna 3 11 identifies transmit antenna 4 [7:4] TXPWR – Index into TxPowerLevels for transmit power level	0(h)
04(h)	RXCHAN	R/W	RXCH - Channel of next received frame [2:0] TFC [2:0] - least significant 3 bits of TFC [5:3] BG[2:0] – 3-bit Band Group [6] TFC[3] – most significant bit of TFC [7] RESERVED (See Reference[1] for the mapping of Channel Number to Band Group and TFC)	0(h)
05(h)	RXCTL	R/W	Receive Control [0] RXPT - Preamble type of next received frame. 0 = Standard Preamble 1 = Burst Preamble [1] PTON (R/W) 0 = PHY does not process PT bit in PLCP header 1 = PHY does process PT bit in PLCP header [3:2] RXANT – Receive antenna to be used. Value 0..SupportedDiversity[1:0] where: 00 identifies receive antenna 1 01 identifies receive antenna 2 10 identifies receive antenna 3 11 identifies receive antenna 4 [7:4] RESERVED	0(h)
06(h)	PMMODE	R/W	[2:0] Power management mode. Values: 0 READY. 1 STANDBY 2 SLEEP Values 3-7 RESERVED [7:3] RESERVED	1(h)
07(h) – 0A(h)	RANGINGTIMER	R	Ranging Timer (units 1/4224MHz) [31:0] RANGINGTIMER - 32-bit ranging counter value. Note that this register requires multiple read operations (07(h) to 0A(h)) to retrieve the full value.	0(h)
0B(h)	CRDExtension	R/W	Extension for 2nd Octet of Regulatory domains [7:0] RESERVED	0(h)

0C(h)	WTONEMAPADDRESS	R/W	Tone Nulling Map Address [3:0] ADDRESS - address used by WTONENULLDATA to select which set of 8 Tone Nulls to be written or read [5:4] BAND - Selected band within the Band Group 00 = Lower band of frequencies in the Band Group 01 = Middle band of frequencies in the Band Group 10 = Upper band of frequencies in the Band Group 11 = Only used when bit 6 is set to 1 to reset the tone nulling map for all band IDs [6] RESET - When set to 1 will reset all tone nulling map values for the band of frequencies selected by WTONEMAPADDRESS[5:4] [7] Reserved Note: Bits [5:0] will auto post increment, wrapping from 0b101111 to 0b000000 on every access to WTONENULLDATA Note: See section 5.2 Tone Nulling in [1]	0(h)
0D(h)	WTONENULLDATA	R/W	Tone Nulling Data [7:0] The value of the 8 tone nulls addressed by WTONEMAPADDRESS. For each bit in WTONENULLDATA 0 = Tone is to be nulled 1 =Tone is not to be nulled (reset value) Note: Every access to this register will cause bit [5:0] of WTONEMAPADDRESS to post increment with wrap.	ff(h)
0E(h)	MPI CONFIG	R/W	MPI interface control [0] Disable Data_Valid signal – when set this will force a DATA_VALID capable PHY to be backward compatible and internally self generate the data valid signal. [1] Enable DDR Mode – when set the data interface is to transfer all data in DDR mode. [2[Enable Parallel Management Interface Mode.	

5.6 Register Map

Figure 5-3 shows the register map. Gray portions in the map are reserved.

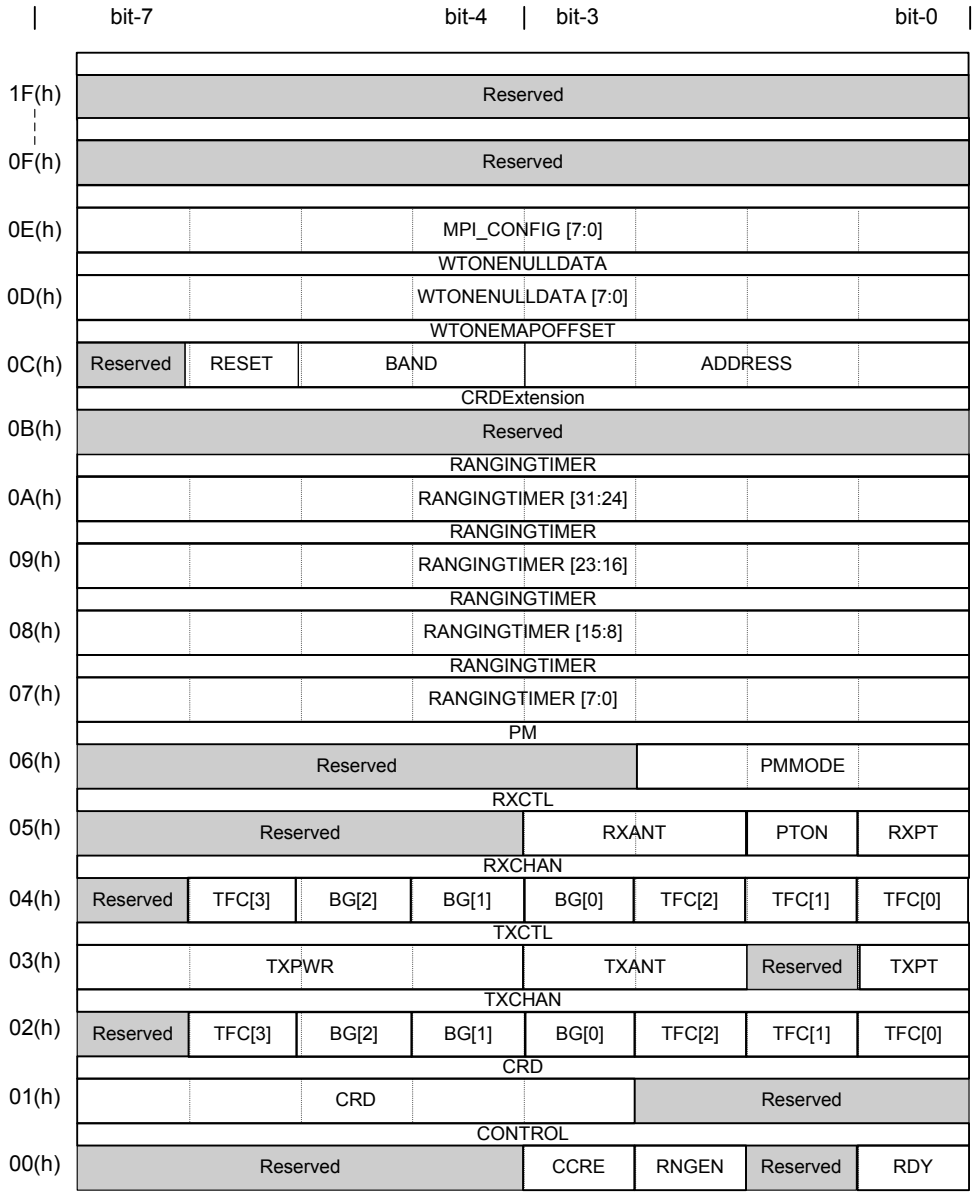


Figure 5-3 Register Map

5.7 Register Set Access Timing

5.7.1 Transmit Control Registers

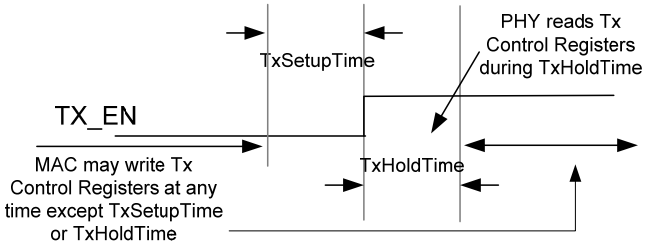


Figure 5-4 Transmit Control Register Setup & Hold

TXCHAN and TXCTL (TXPT, TXANT and TXPWR) are registers used to specify parameters for the next transmit frame operation. They shall be set by the MAC at least TxSetupTime PCLK cycles before the assertion of TX_EN and are held stable for at least TxHoldTime PCLK cycles. The PHY shall read these registers within this TxHoldTime period. The values of these registers then control the parameters for the transmit frame operation corresponding to this TX_EN assertion.

5.7.2 Receive Control Registers

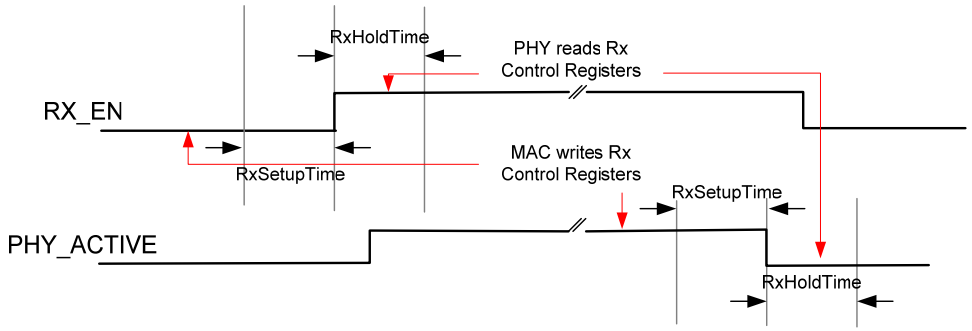


Figure 5-5 Receive Control Register Setup & Hold

RXCHAN and RXCTL (RXPT and RXANT) are registers used to specify parameters for the next receive frame operation. They shall be set by the MAC at least RxSetupTime PCLK cycles before the assertion of RX_EN and are held stable for at least RxHoldTime PCLK cycles. The PHY shall read these registers in this RxHoldTime period ignoring any PTON setting and any previous BM or PT settings. The values of these registers then control the parameters for the receive frame operation corresponding to this RX_EN assertion.

For burst mode reception, the MAC shall set the registers for the next receive frame operation at least RxSetupTime PCLK cycles before PHY_ACTIVE de-assertion indicating the end of frame reception. The PHY shall read the registers within RxHoldTime PCLK cycles following the de-assertion of PHY_ACTIVE. These registers then control the parameters for the reception of the next frame if RX_EN is not de-asserted. In receive burst mode (see Section 7.8.3) PTON together with the BM and PT bits of the preceding frame's PLCP header may override the RXPT register setting.

RX_EN de-assertion and re-assertion has precedence over PHY_ACTIVE de-assertion and will cause the PHY to overwrite any internal values loaded from the receive control registers.

Table 5-3 Register Access Parameter Values

PARAMETER	MINIMUM VALUE (PCLK PERIODS)	MAXIMUM VALUE (PCLK PERIODS)
TxSetupTime	0	128
TxHoldTime	0	128
RxSetupTime	0	128
RxHoldTime	0	128

5.8 Tone Nulling Map Control

At any time respecting the setup and hold timings, the MAC may write the tone nulling information to the PHY. WTONEMAPADDRESS and WTONENULLDATA are not Transmit Control or Receive Control registers and do not require double buffering. The protocol for writing the tone nulling information is an address followed by data protocol with auto address post increment.

Writing WTONEMAPADDRESS sets the address pointer in the PHY to the data location of the first tone to be accessed. Subsequent read/writes to WTONENULLDATA will retrieve/update the tone nulling information of 8 tones per access while post incrementing the address pointer in the PHY. Setting bits to '0' indicates that the tone is to be nulled.

Table 5-4 Tone Nulling Mapping to PHY Parameters

WTONEMAPADDRESS		FREQUENCY	
bit [5:4] BAND	bit [3:0] ADDRESS	Band in Band Group	Subcarriers (LSB .. MSB)
0b00	0b0000	Lower	-64..-57
0b00	0b0001	Lower	-56..-49
..	..	..	..
0b00	0b1111	Lower	56..63
0b01	0b0000	Middle	-64..-57
..	..	..	..
0b10	0b0000	Upper	-64..-57
..	..	..	..

As illustrated in Table 5-4, subcarrier ordering is from {-64,…-1,0,1,…63} for each band, starting with the lowest frequency band in the band group.

The entire tone nulling map or just the portion of the map associated with a particular band ID can be reset using bit [6] of WTONEMAPADDRESS along with bits [5:4] to identify the area to be reset. Tone nulls are reset to '1' indicating that they are not to be nulled.

6 Frame Structures

According to the WiMedia PHY specification (Referenced Document [1]), data is transmitted and received least-significant bit first (bit zero octet zero … bit 7 octet zero, bit 0 octet 1 … bit 7 octet 1 etc.). Consequently, the PLCP header, as shown in Figure 6-2, is presented to DATA[7:0] as shown in Figure 6-1.

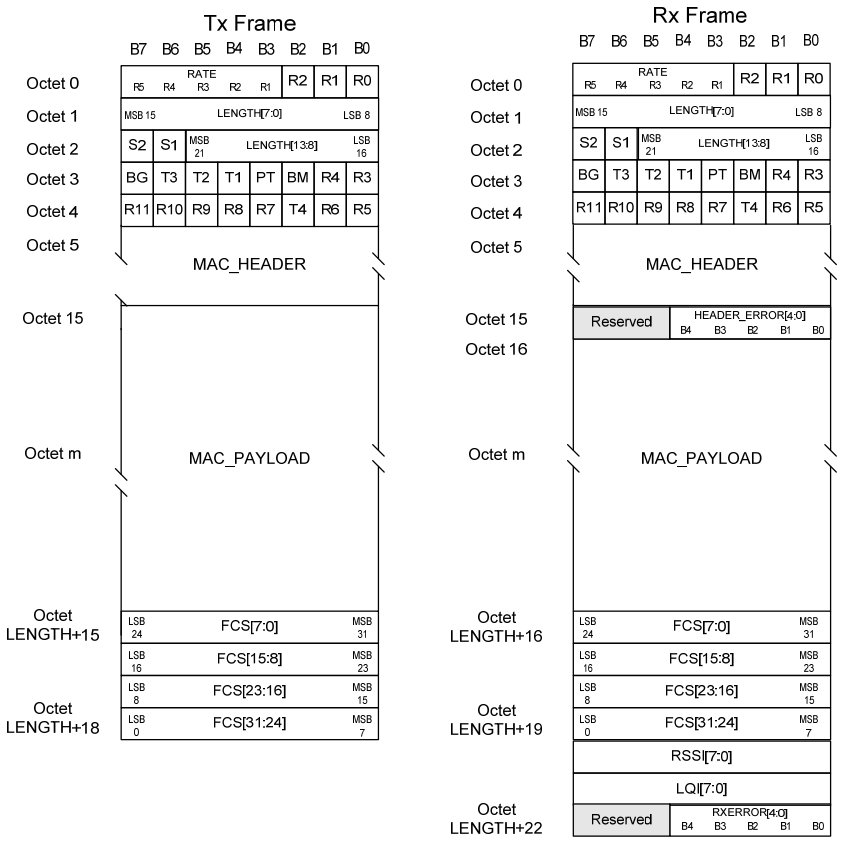


Figure 6-1 Frame Structures for Transmit & Receive States

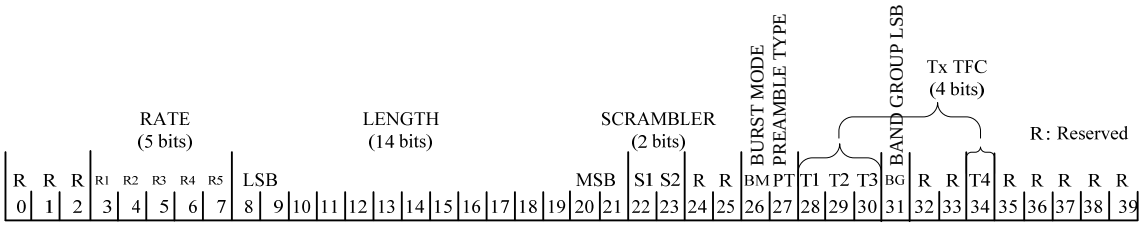


Figure 6-2 PLCP Header Format

The MAC_HEADER, MAC_PAYLOAD and FCS are presented to the PLCP as defined in the WiMedia MAC specification [2]. As defined in that specification, the coefficients ($a_{31}...a_0$) of the CRC result polynomial

$$a_{31}x^{31}+ a_{30}x^{30}+ a_{29}x^{29}+ a_{28}x^{28}+ a_{27}x^{27}.....+a_7x^7+ a_6x^6+ a_5x^5+ a_4x^4+ a_3x^3+ a_2x^2+ a_1x+ a_0$$

are mapped to the bits of the FCS as shown in Figure 6-3 and presented to the PLCP as shown in Figure 6-1.

bits: b31	b30	b29	…	b2	b1	b0
a0	a1	a2	…	a29	a30	a31

Figure 6-3 FCS Field format

Thus when presented to the PLCP least significant octet first (FCS[7:0]) the coefficients of the CRC are transmitted in the order $a_{31..}$ $a_{0.}$

The following TxFrame control bits (see Figure 6-2) shall be set by the MAC in all transmitted frames and shall be delivered to the MAC by the PHY in the RxFrame format of all received frames:

- RATE is the data rate at which the MAC Frame Payload is transmitted. If LENGTH = 0, RATE shall be set to '00000';
- LENGTH is the MAC Frame Payload length in octets excluding the FCS octets. If LENGTH is zero, the FCS field is not present;
- SCRAMBLER is set to zero during initialization of the PHY or after any !PHY_RESET. The unsigned binary integer set in SCRAMBLER is incremented by the MAC, modulo 4, for each frame transmitted from the MAC to its PHY;
- BM and PT shall be set in all transmitted frames according to the rules defined in Section 7.6;
- The MAC sets TX_TFC and BG as derived from TXCHAN (see Table 5-2) in all transmitted frames.

Table 6-1 Tx Frame Fields

FIELD	BITS	DESCRIPTION
R0, R1, R2, R3, R4, R5, R6, R7, R8, R10, R11	1	RESERVED bits; shall be set to 0 on transmit.
RATE	5	Indication of transmit data rate of MAC Frame Payload Rate (Mbps) [R1:R5] 53.33 00000 80 00001 106.67 00010 160 CC 00011 200 CC 00100 320 CC 00101 400 CC 00110 480 CC 00111 640 01000 800 01001 960 01010 1024 01011 Reserved 01100-10010 160 LDPC 10011 200 LDPC 10100 320 LDPC 10101 400 LDPC 10110 480 LDPC 10111 Reserved 11000 - 11111

LENGTH	14	Length of the MAC frame payload (unit: octet) 14-bit unsigned binary integer lsb 8 --- msb 21
SCRAMBLER	2	Scrambler initialization bits S1 and S2
BM	1	Burst Mode bit (Interframe Space following this frame) 0 = Normal Mode (SIFS or other) 1 = Burst Mode (MIFS) (Note: SIFS = pSIFS, MIFS = pMIFS, as defined in [1])
PT	1	Preamble type of the frame following this frame 0 = Standard Preamble 1 = Burst Preamble
TX_TFC	4	TF Code used at the transmitter TF Code T1-T4 1 1000 2 0100 3 1100 4 0010 5 1010 6 0110 7 1110 8 0001 9 1001 10 0101 Reserved 0000 Reserved 1101 Reserved 0011 Reserved 1011 Reserved 0111 Reserved 1111
BG	1	Least-significant bit of the BAND GROUP used at the transmitter Band Group BG 1, 3, 5 1 2, 4, 6 0
MAC_HEADER	80	MAC Frame header
MAC_PAYLOAD	---	Frame Data
FCS	32	Frame FCS

Table 6-2 Rx Frame Fields

FIELD	BITS	DESCRIPTION
R0, R1, R2, R3, R4, R5, R6, R7, R8, R10, R11, R12, R13, R14, R15, R16, R17	1	RESERVED bits; shall be ignored on receive.

RATE	5	Same as Tx Frame Fields
LENGTH	14	Same as Tx Frame Fields
SCRAMBLER	2	Scrambler initialization bits S1 and S2.
BM	1	Burst Mode bit indicates the Inter-Frame Space following this receive frame 0 = Normal IFS (Depends on MAC context) 1 = Burst Mode IFS (MIFS) (Note : SIFS = pSIFS MIFS = pMIFS as defined in [1])
PT	1	Preamble Type for the frame following this frame 0 = Standard Preamble 1 = Burst Preamble
TX_TFC	4	Same as Tx Frame Fields
BG	1	Same as Tx Frame Fields
MAC_HEADER	80	Same as Tx Frame Fields
HEADER_ERROR	5	Immediate Header Error reporting. Error is indicated by the corresponding bit set to 1. bit 0: RESERVED bit 1: RESERVED bit 2: WRONG_CHANNEL bit 3: UNSUPPORTED_RATE bit 4: HCS_ERROR All bits = “0” represents “NO_ERROR”
MAC_PAYLOAD	---	Same as Tx Frame Fields
FCS	32	Same as Tx Frame Fields
RSSI	8	Receive power estimate of received signal
LQI	8	Quality estimate of received signal
RXERROR	5	Receiving results of Rx frame Each bit represents the cause of error bit 0: PAYLOAD_ERROR bit 1: RESERVED bit 2: WRONG_CHANNEL bit 3: UNSUPPORTED_RATE bit 4: HCS_ERROR All bits = “0” represents “NO_ERROR”

7 Interface Theory of Operation

7.1 Overview

A simplified PHY state diagram is shown in Figure 7-1.

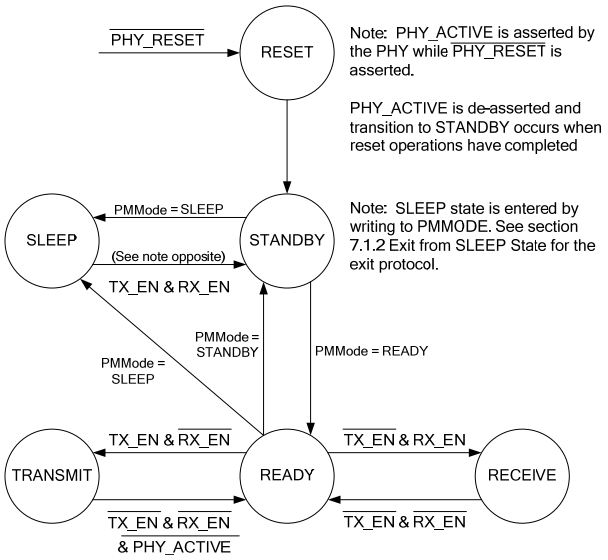


Figure 7-1 PHY State Transition Diagram

7.1.1 PHY Reset Protocol

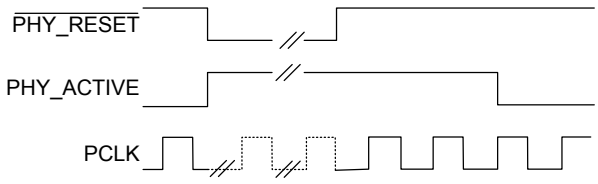


Figure 7-2 PHY Reset Protocol

At any time and from any PHY state including after initial power on, the MAC may force the PHY into RESET state by asserting control signal !PHY_RESET. The PHY indicates entry to RESET state by asserting PHY_ACTIVE and optionally stopping PCLK. Transitions on both !PHY_RESET and PHY_ACTIVE in this case are asynchronous to PCLK.

During reset, the PHY drives CCA_STATUS, DATA_EN and DATA[7:0] to their inactive values. The MAC drives RX_EN, TX_EN and SERIAL_DATA to their inactive values. PHY_ACTIVE is driven as described above.

The MAC maintains !PHY_RESET asserted for at least PHY specific interval PHYResetTime. After !PHY_RESET is de-asserted the PHY completes its reset operations. When PCLK is stable (according to PHY specific conditions) the PHY de-asserts PHY_ACTIVE to indicate transition to STANDBY state. The PHY is responsible for setting PMMODE to STANDBY and RDY to the appropriate value. If RDY is set by the PHY to indicate abnormal completion of RESET operation, the meaning of all registers except RDY is undefined.

7.1.2 Exit from Sleep State

The MAC may place the PHY into SLEEP state by writing SLEEP to the PMMODE register (see Table 5-2). During SLEEP state, the PHY reduces power consumption by turning unnecessary functions off. However, the contents of the Dynamic Registers are maintained

through SLEEP and can be assumed unchanged after the PHY is returned to STANDBY state.

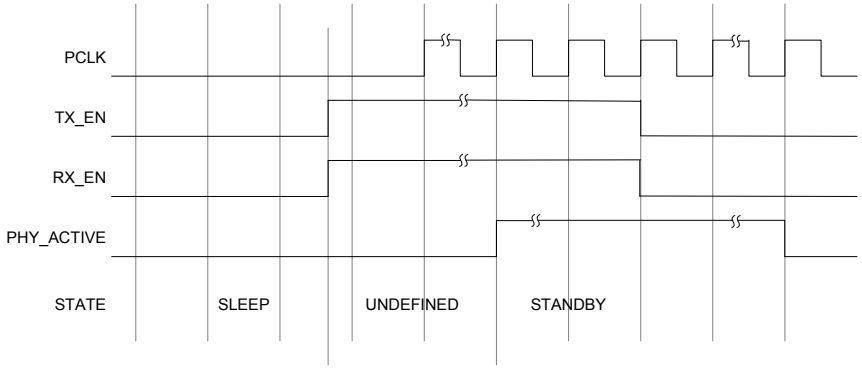


Figure 7-3 Exit SLEEP protocol

Exit from SLEEP state is carried out by the following operations:

- The MAC asserts both TX_EN and RX_EN
- When the PHY has reached STANDBY state, it asserts PHY_ACTIVE and sets PMMODE to STANDBY
- When the MAC detects the rising edge of PHY_ACTIVE, it de-asserts TX_EN and RX_EN
- The PHY responds by de-asserting PHY_ACTIVE.

7.1.3 Normal Operation

By writing to the PHY configuration register PMMODE (see Section 5), the MAC controls transitions between any two of the three PHY states: SLEEP, STANDBY and READY except for transitions from SLEEP state which requires a special operation as described in Section 7.1.2.

When the PHY is not actively transmitting or receiving, it will normally be in STANDBY state. In preparation for an active time period, the MAC must first put the PHY in READY state by writing into configuration register PMMODE. The MAC must put the PHY in READY state at least TurnOnDelay microseconds before commanding the PHY into TRANSMIT or RECEIVE state. After this delay, TRANSMIT or RECEIVE state can be initiated by the MAC asserting TX_EN or RX_EN respectively. The PHY is returned to READY state by de-asserting the same signal. (For complete transition conditions, see Transmit and Receive subsections later in this chapter.) Once the PHY is back in READY state, the MAC may either initiate another frame transmission or reception by again asserting TX_EN or RX_EN, or it may command the PHY back into STANDBY by writing to register PMMODE.

Table 7-1 gives the complete conditions for the PHY state transitions.

Table 7-1 State Transition Conditions

TRANSITION	TX_EN	RX_EN	WRITE TO PMMODE
RESET → STANDBY	LOW	LOW	—
STANDBY → SLEEP	LOW	LOW	SLEEP
SLEEP → STANDBY	HIGH	HIGH	—
STANDBY → READY	LOW	LOW	READY
READY → SLEEP	LOW	LOW	SLEEP
READY → STANDBY	LOW	LOW	STANDBY
READY → TRANSMIT	Rising edge	LOW	—
TRANSMIT → READY	Falling edge	LOW	—
READY → RECEIVE	LOW	Rising edge	—
RECEIVE → READY	LOW	Falling edge	—

7.2 Frame Timing

Precise frame timing is provided by the MAC (except when in Burst Mode as described in 7.7.3) for transmit operations and by the PHY/MAC for receive operations.

- Start of transmitted frame timing is indicated by the rising edge of TX_EN associated with the PHY-dependent, but fixed, PHY transmit processing delay TxDelay for single frame transmission and for the 1st frame of a Burst transmission
- End of transmit frame timing is indicated by the falling edge of PHY_ACTIVE
- Start of receive frame timing is indicated by the rising edge of PHY_ACTIVE associated with the PHY-dependent, but fixed, PHY receive processing delay SyncDelay
- End of receive frame timing is indicated by the falling edge of PHY_ACTIVE associated with the PHY-dependent, but fixed, PHY receive delay PhyActiveDelay.

7.3 Ranging Support

Ranging estimation may be optionally supported by the PHY. Capabilities are indicated by static parameter RangingSupported. If ranging is supported, timing of transmission and reception events may be controlled via the RNGEN bit [2] in the CONTROL [00h] dynamic parameter register.

PHYs which support ranging must provide up to a 32-bit ranging counter and indicate the precision of the timestamp by reference to the frequency of the ranging counter.

RNGEN is to indicate whether the PHY should set the RANGINGTIMER register from the ranging counter during transmission and reception.

The interface events associated with these timestamps are:

- The start of transmission of the preamble at the local antenna as indicated by the assertion of PHY_ACTIVE
- The acquisition of the preamble as indicated by the assertion of PHY_ACTIVE during reception.

These transitions on PHY_ACTIVE provide support for ranging procedures which may be implemented within or above the MAC by indicating when ranging timestamps should be retrieved. However, the ranging timestamp value is not tied to the PCLK timing associated with PHY_ACTIVE transitions. See the ranging section in Reference [1] for definition of the ranging timestamp reference, and associated calibration parameters RANGING_TRANSMIT_DELAY and RANGING_RECEIVE_DELAY.

The processing of the timestamps by the MAC or higher layer functions is outside the scope of this specification. The Two-Way Time Transfer range measurement mechanism defined in Referenced Documents [2] uses the following MAC-PHY interface registers and parameters:

- RANGINGTIMER;
- RangingSupported,
- RANGING_TRANSMIT_DELAY,
- RANGING_RECEIVE_DELAY;
- PHYClockAccuracy.

Calculation details are described in Reference [2].

7.4 Transceiver Delay Definitions

Figure 7-4 and Figure 7-5 show the principle transceiver delay intervals for Transmit and Receive cases respectively.

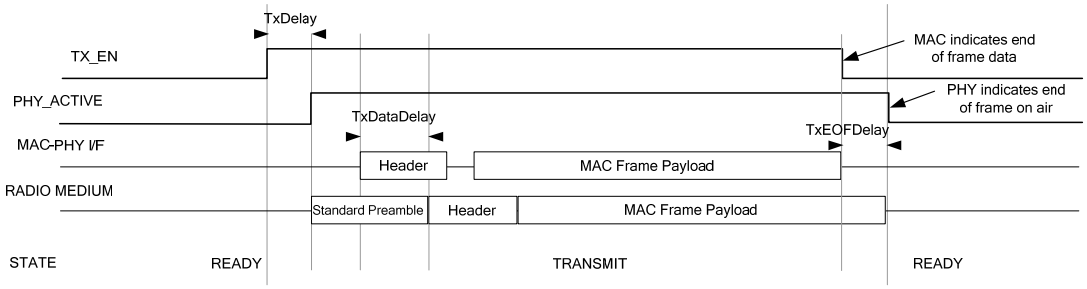


Figure 7-4 Transmit Delay Intervals

TxDelay is the interval between the assertion of TX_EN and the start of the first symbol of the preamble being present at the local antenna.

The PHY requests header data by asserting DATA_EN no earlier than TxDataDelay before the end of the preamble as shown in Figure 7-4. TxDataDelay is measured backwards from the end of the preamble to provide a fixed, preamble independent, header processing interval for PHY implementations and a fixed interval between TX_EN assertion and the first assertion of DATA_EN to be used by the MAC for end of previous frame processing.

The MAC must drive valid data to DATA[7:0] and assert DATA_VALID 2 PCLK periods after DATA_EN is asserted to maintain MPI version 1.2 backward compatibility.

The PHY requests the last octet of data by asserting DATA_EN not less than TxEOFDelay before de-asserting PHY_ACTIVE.

The PHY de-asserts PHY_ACTIVE on the rising edge of the PCLK following the transmission of the end of the last symbol of the frame at the local antenna.

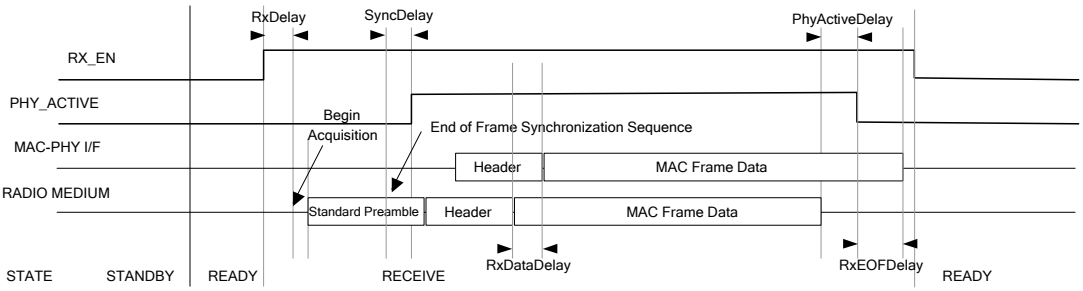


Figure 7-5 Receive Delay Intervals

RxDelay is the interval between the assertion of RX_EN and the start of the preamble acquisition operation by the PHY.

Precise start of frame timing is provided by the PHY via the assertion of PHY_ACTIVE a PHY-dependent but fixed delay, SyncDelay, after the end of last symbol of the preamble Frame Synchronization Sequence (preceding the Channel Estimation Sequence) arrives at the local antenna.

The PHY transfers the HEADER_ERROR octet across the MAC-PHY Interface no later than RxDataDelay after the end of the PLCP header at the local antenna.

End of frame timing is provided by de-assertion of PHY_ACTIVE a PHY-dependent, but fixed, delay, PHYActiveDelay, after the end of the last symbol is received at the local antenna. PHYActiveDelay compensates for the processing delay inherent in the PHY receive processing path. The PHY transfers the last octet of the frame across the MAC-PHY Interface no later than RxEOFDelay after de-asserting PHY_ACTIVE.

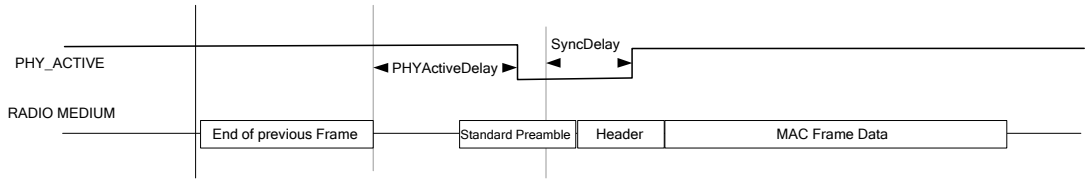


Figure 7-6 PHYActiveDelay Timing

As shown in Figure 7-6, PHYActiveDelay may overlap with the start of the preamble of the next receive frame but must permit PHY_ACTIVE to be de-asserted before the end of the Frame Synchronization sequence to permit acquisition of the incoming frame to be signaled. It is the responsibility of the PHY vendor to specify the value of PHYActiveDelay such that this condition can be met for a zero length frame.

Precise end of frame timing can also be calculated from the known precise start of frame timing, preamble, PHY Header and MAC Frame Data structures, data rates and symbol encoding.

7.5 Transceiver Turnaround Times

7.5.1 Rx-Tx Turnaround Time

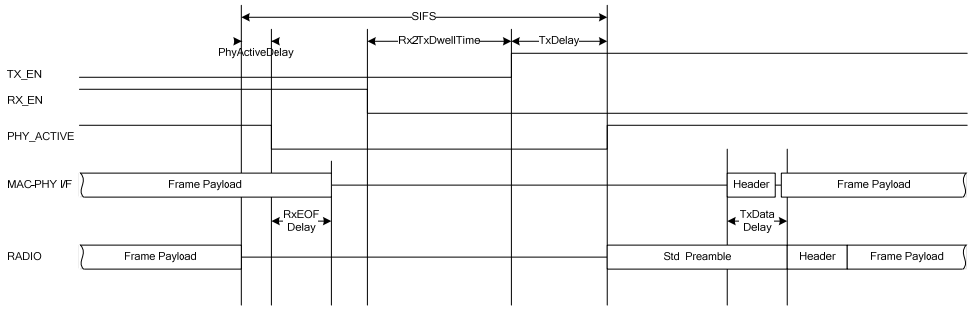


Figure 7-7 Rx-Tx Turnaround Time

The minimum interval between RX_EN de-assertion and TX_EN assertion shall be a fixed, PHY specific value, Rx2TxDwellTime. The following inequality shall be respected:

PHYActiveDelay + RxEOFDelay + Rx2TxDwellTime + TxDelay < SIFS

7.5.2 Tx-Rx Turnaround Time

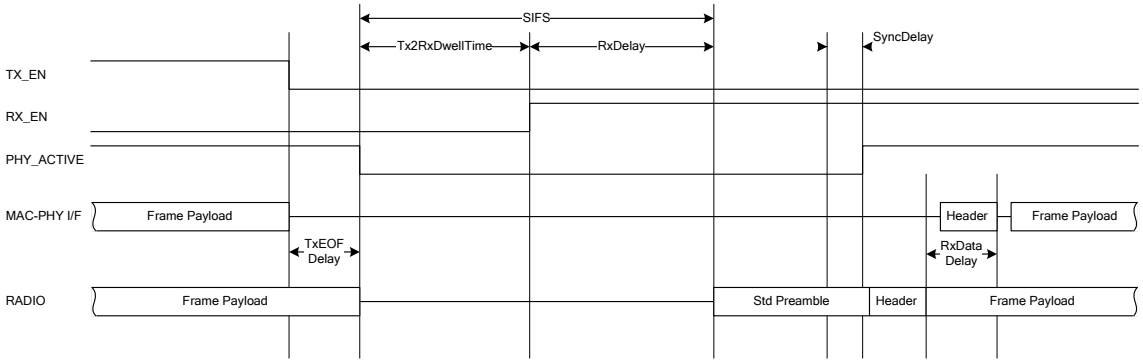


Figure 7-8 Tx-Rx Turnaround Time

The minimum interval between PHY_ACTIVE de-assertion (in TRANSMIT State) and RX_EN assertion shall be a fixed, PHY specific value, Tx2RxDwellTime. The following inequality shall be respected:

Tx2RxDwellTime + RxDelay < SIFS

7.6 Preamble Control

7.6.1 Single Frame Transmission and Reception

In each single frame transmission the Standard Preamble is transmitted.

- BM shall be set to ‘0’ for single frame transmission
- PT shall be set to ‘0’ for single frame transmission

In single frame reception, the preamble to be acquired by the receiver is defined by register RXPT which must be set, respecting the receive setup and hold times defined in 5.7.2, to indicate the Standard Preamble.

7.6.2 Burst Mode Transmission

A burst is defined as a MIFS separated sequence of frames (see 7.7.3). In burst transmission, the PHY assures the accurate MIFS timing between frames. The preamble to be transmitted with each frame is defined by the rules summarized below:

- BM shall be set to 1 for Burst Mode frame transmission.

7.6.2.1 Data Rates of 200 Mbps or Lower

For DATA RATES of 200Mbps or lower, all frames in the burst shall use the Standard Preamble.

- PT shall be set to '0' for data rates of 200Mbps or lower

7.6.2.2 Data Rates above 200 Mbps

For DATA RATES above 200Mbps, the first frame in the burst shall use the Standard Preamble. The second and subsequent frames of the burst may use the Burst Preamble or the Standard Preamble.

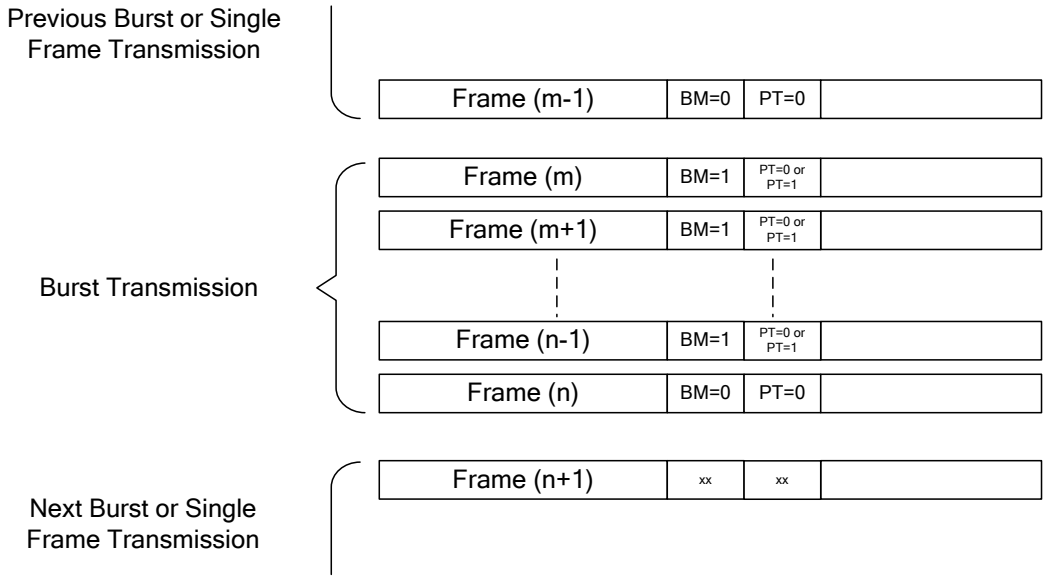


Figure 7-9 Burst transmission preamble control

As shown in Figure 7-9 a burst transmission begins with a frame (m) carrying BM = '1' in the PLCP Header, normally preceded by a frame (m-1) with BM = '0' and PT = '0'.

- The 1st frame in the burst (frame m) is transmitted with the Standard Preamble.
- The 2nd and subsequent frames (m+1,…, n) of the burst are transmitted with a preamble type defined by PT in the preceding (m,…, n-1) frame PLCP Header.
- The last frame (n) in the burst is transmitted with BM = '0' and PT = '0'.

7.6.3 Burst Mode Reception

In burst mode reception the MAC maintains RX_EN asserted between frames within the burst.

During burst mode reception, processing of PT when BM = '1' is performed automatically by the PHY when register PTON is set to '1'.

The MAC is responsible for all receive preamble control via register RXPT when register PTON is set to '0'.

A burst mode reception is terminated following reception of a frame with BM = ‘0’ or immediately after RX_EN is de-asserted.

7.7 Transmit Operation

There are two transmit operations – Single Frame transmit and Burst Mode transmit. The DATA bus can be configured to transfer data in either Single byte per cycle mode (SDR) or Double byte per cycle mode (DDR).

In single frame transmission, a single frame is transferred from the MAC to the PHY and on-air timing is controlled by the state of TX_EN and the PHY transmission of symbols at the local antenna. There is no specific operation following completion of the single frame transmission. The next operation could be another transmit operation, a receive operation, or transition to STANDBY.

In Burst Mode Transmit there is an explicit relationship between each frame in a sequence of frames. On-air timing is controlled by TX_EN for the start of the first frame only. Subsequent frame timing is maintained by the PHY during the burst.

Data transfer is by default performed in Single byte per cycle mode (SDR). If the PHY is DDR capable (indicated in MPI Capability Static Register) it can be placed in DDR mode by the MAC by writing to the PHY’s MPI_CONFIG dynamic register. In DDR mode the DATA is transferred on both rising and falling edges of MCLK.

7.7.1 Data Bus Ownership

The DATA[7:0] bus is driven by the MAC in TRANSMIT state and by the PHY in RECEIVE state. The owner of the bus for the remaining states depends on the mode of the Management interface. The rules are as follows:

In Serial Management mode the PHY owns the bus for all states except for TRANSMIT state. The MAC shall take control of DATA[7:0] three clocks following TX_EN assertion. The MAC shall relinquish control two clocks after TX_EN de-assertion regardless of the PHY requesting data by asserting DATA_EN.

In Parallel Management mode the MAC owns the bus for all states except for RECEIVE state. The PHY shall take control of DATA[7:0] three clocks following RX_EN assertion. The PHY relinquishes control two clocks after RX_EN_FINISH de-assertion (see section 7.13.2 for definition of RX_EN_FINISH).

7.7.2 Single Frame Transmission Control

The MAC has complete control over the single frame transmission operation. For each frame transmitted, the MAC sets the PLCP Header parameters listed in Table 7-2 in the Tx Frame format as defined in Figure 6-1.

The MAC also sets the Transmit control registers listed in

Table 7-3 respecting the setup and hold times defined in Figure 5-4.

Table 7-2 Single Frame Transmit Parameters

PARAMETER	VALUE	COMMENT
SCRAMBLER	$\|(S1..S2) + 1\|_4$	S1 & S2 are treated as a 2-bit unsigned integer and incremented for each frame sent from the MAC to the PHY
BM	0	Burst Mode is always 0 for single frame transmissions
PT	0	Preamble Type is always 0 for single frame transmission
TX_TFC	T1..T4	TFC code used to transmit the frame
BG	BG LSB	Least-significant bit of Band Group
RATE	00000 …. 01011 10011 …. 10111	Encoding of data rate and coding scheme for the MAC frame payload. Value shall be set to 00000 if LENGTH is zero.
LENGTH	0…16383	Number of Octets in MAC Frame Payload part of Frame

Table 7-3 Transmit Control Registers for Single Frame Transmit

REGISTER	VALUE	COMMENT
TXCHAN	Valid Channel	Channel on which to perform the transmit operation; see Section 7.2 of Reference [1].
TXCTL-TXPT	0	The preamble is always the Standard Preamble in single frame transmissions
TXCTL-TXANT	0.. SupportedDiversity[5:4]	Identifies the transmit antenna
TXCTL-TXPWR	0.. NumTxPwrLevels	Transmit power level index
CONTROL-RNGEN	0 1	If RangingSupported = 0 RNGEN is set to 0 If RangingSupported = 1 RNGEN is set to 0 to disable RANGINGTIMER setting RNGEN is set to 1 to enable RANGINGTIMER setting
MPI_CONFIG	0 1	If MPI_CONFIG[1] = 0 all transmit operations are performed in SDR Single Byte per Cycle mode. If MPI_CONFIG[1] = 1 all transmit operations are performed in DDR mode.

Figure 7-10 illustrates the transmission of a single frame in SDR mode, starting from READY state. The MAC starts the transmission by asserting TX_EN while keeping RX_EN low. When the PHY detects the rising edge of TX_EN it transitions to TRANSMIT state, turns on the radio transmit path and begins to transmit the preamble defined by TXPT using its antenna defined by TXANT on the channel defined by TXCHAN.

The timing of TX_EN assertion should be TxDelay ahead of nominal frame timing at the local antenna to compensate for PHY transmit processing delay.

In TRANSMIT State the PHY has full control over data flow. Data is requested from the MAC by asserting DATA_EN at the rising edge of PCLK. The MAC must drive DATA[7:0] and DATA_VALID 2 clock cycles later to maintain backward compatibility with earlier versions of the MPI interface.

Figure 7-11 illustrates the same single frame as shown in figure 7-10 in DDR mode.

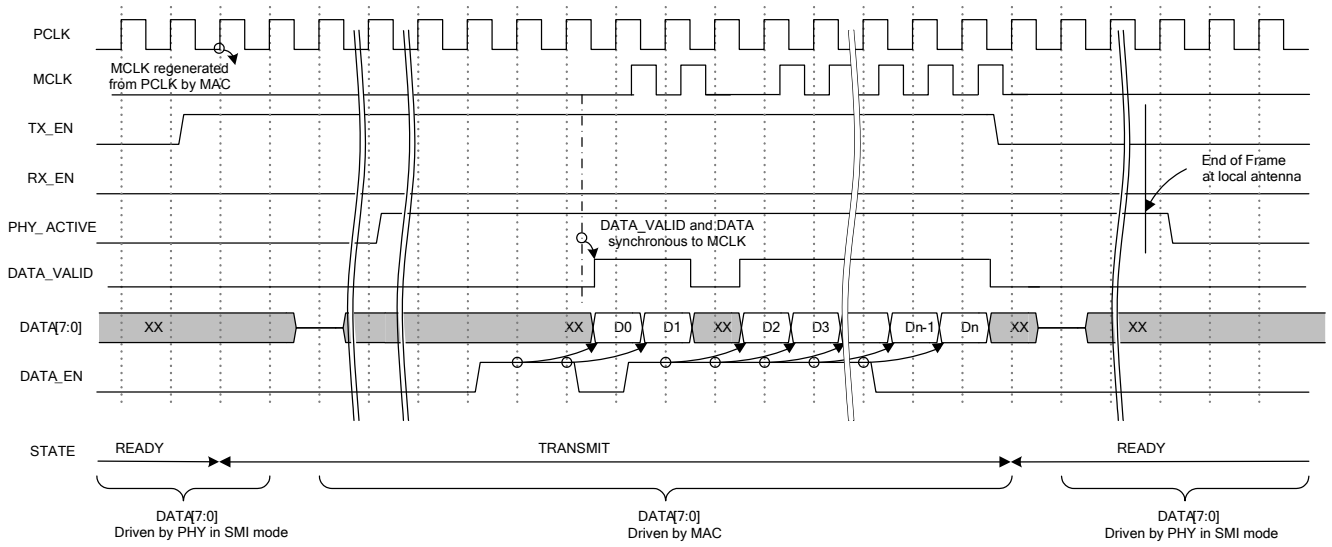


Figure 7-10 Single Frame Transmit Timing SDR Mode

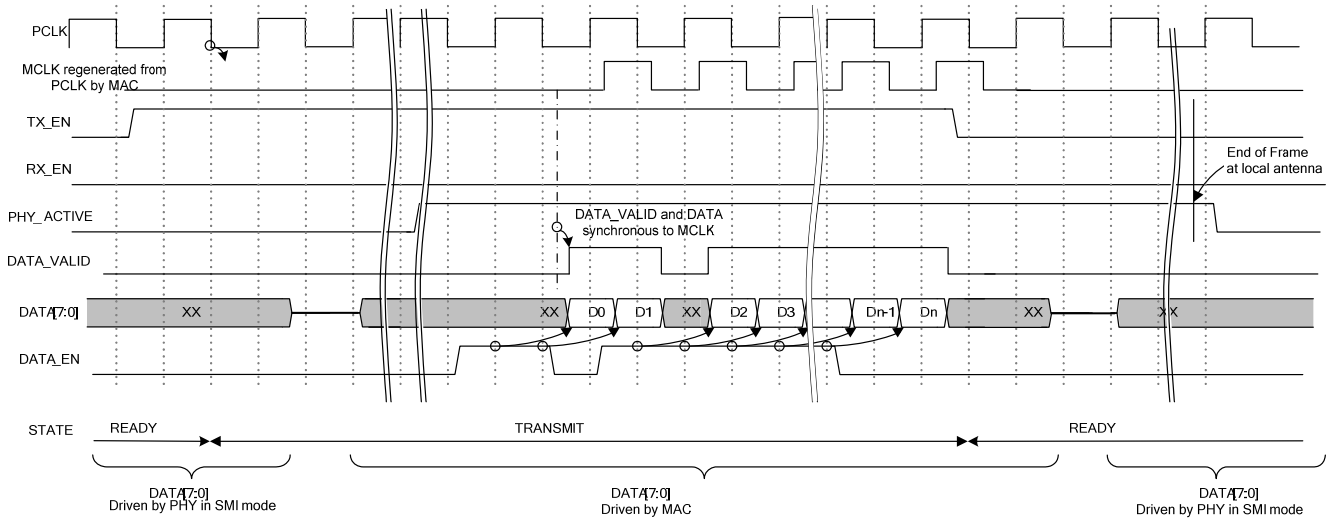


Figure 7-11 Single Frame Transmit Timing DDR mode

The PHY performs the following operations:

- Asserts PHY_ACTIVE at the rising edge of PCLK following the transmission of the leading edge of the first symbol of the preamble at the local antenna
- If RNGEN = 1 sets Dynamic Register RANGINGTIMER at the Ranging Reference Signal (defined in the ranging section of Reference [1] as the first sample of the first Channel Estimation Sequence of the preamble) according to the precision defined by the Ranging Supported static parameter (see Table 5-1)
- Requests Header and Payload data (as appropriate) from the MAC by asserting DATA_EN while respecting TxDataDelay.

The MAC performs the following operations:

- Transfers one octet of header or payload data (as appropriate) for each request from the PHY via the assertion of DATA_EN. In SDR mode DATA_EN is valid on the rising edge of PCLK. In DDR mode DATA_EN is valid on both rising and falling edges of PCLK. Each valid byte from the MAC is accompanied with the DATA_VALID signal asserted. The DATA_VALID and DATA signals are synchronous to the MCLK signal. Data is transferred only on the rising edge for SDR and both edges for DDR mode.
- Completes the transmit operation by de-asserting TX_EN at the rising edge of the MCLK cycle after the last octet of the frame FCS (or MAC Header if LENGTH is zero) has been transferred to the PHY.
- MCLK is the regeneration of the PCLK signal used to make DATA source synchronous. It shall be active at minimum when TX_EN and PHY_ACTIVE are both asserted plus 1 cycle after the last byte is clocked out of the MAC. MCLK may be active at other times but the PHY shall not rely on it for correct functioning of the TX interface during those times.

The PHY completes the single frame transmit operation by:

- De-asserting PHY_ACTIVE at the rising edge of PCLK following the transmission of the trailing edge of the last symbol from the local antenna
- Transitioning back to READY state

This procedure is repeated for each transmitted frame. The MAC is responsible for calculating the start of frame timing in all cases.

A frame transmission can be aborted by the MAC at any time by de-asserting TX_EN before the last octet of the FCS (or MAC Header if LENGTH is zero) has been transferred to the PHY (see 7.9).

7.7.3 Burst Mode Transmission Control

A burst is a sequence of MIFS separated frames transmitted from the same source. In burst mode transmission, the MAC has control over the timing of the first frame in the sequence of burst mode frames. The first frame is transmitted in exactly the same manner as a single frame transmission, as described in Section 7.7.2, except for the PLCP Header parameters listed in Table 7-4.

Table 7-4 Unique Burst Mode PLCP Header parameters

PARAMETER	VALUE	COMMENT
BM	1	Burst Mode must be set to 1 in the first frame of the burst mode sequence
PT	0	PT = 0 if the next frame will be sent using the Standard Preamble
	1	PT = 1 if the next frame will be sent using the Burst Preamble
LENGTH	1…16383	Number of Octets in MAC Frame Payload part of Frame

Timing for the transmission of subsequent frames in the burst is maintained by the PHY provided that TX_EN is re-asserted within the window shown in Figure 7-12. The minimum duration TX_EN shall remain de-asserted before re-assertion is three PCLK cycles.

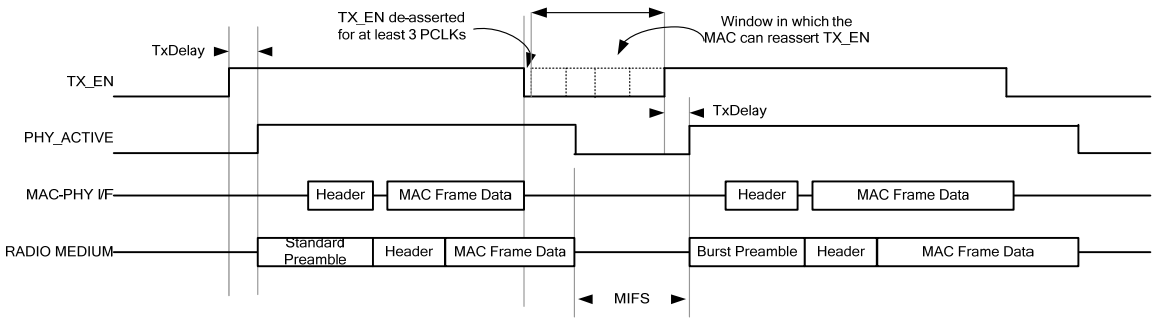


Figure 7-12 Burst Mode Transmission

If the MAC re-asserts TX_EN in this window, the PHY assures the start of the first symbol of the preamble of the next frame is presented at the local antenna exactly MIFS after the end of the last symbol of the previous frame. The MIFS interval is defined to be an exact number of symbols to enable the receiver to maintain synchronization from the Burst Preamble.

In burst transmission, the value of PT overrides TXPT in determination of which preamble the PHY transmits ahead of each PLCP header and MAC frame body (if present).

Each subsequent frame in the burst mode sequence is transmitted as in the single frame case, except for the PLCP Header parameters in Table 7-4 and the assurance of the MIFS interval provided TX_EN is re-asserted within the window defined in Figure 7-12, until the last frame in the sequence, which differs in the PLCP parameters, as defined in Table 7-5.

Table 7-5 Unique Final Frame PLCP parameters

PARAMETER	VALUE	COMMENT
BM	0	Burst Mode must be set to 0 in the last frame of the burst mode sequence
PT	0	PT must be set to 0 in the last frame of the burst mode sequence
RATE	00000 … 01011 10011…10111	Encoding of data rate for the MAC Frame Payload part of the frame. Value shall be set to 00000 if LENGTH is zero.
LENGTH	0 … 16383	Number of Octets in MAC Frame Payload part of Frame. Note the special case of a frame with LENGTH of zero is permitted since the MIFS interval will not be used following this frame.

7.7.4 Burst Mode Transmit Error Recovery

If TX_EN is re-asserted:

- later than TxDelay before MIFS, but earlier than MIFS, after the end of the previous frame, the behavior of the PHY is undefined.
- later than MIFS after the end of the previous frame, the PHY shall abort burst mode transmission and return to normal transmission. The next assertion of TX_EN will be treated as a single frame transmission or the first frame of a new burst mode transmission.

7.8 Receive Operation

7.8.1 Data Bus Ownership

The DATA[7:0] bus is driven by the PHY in RECEIVE state. If not programmed for Parallel Management Interface mode the bus is driven by the PHY in all non-TRANSMIT modes. Valid data is indicated by DATA_EN being asserted at the rising edge of PCLK. IF in DDR mode the falling edge of PCLK is also used to transfer valid data.

7.8.2 Single Frame Reception Control

The MAC has control over frame reception operations via the RX_EN control signal. For each frame received, the MAC sets the Receive control registers listed in Table 7-6 respecting the setup and hold times defined in Figure 5-5. The PHY reports the received PLCP Header parameters in the receive frame format as described in Figure 6-1.

Table 7-6 Receive Control Registers for Single Frame Receive

REGISTER	VALUE	COMMENT
RXCHAN	Valid channel	Channel on which to perform the receive operation; see Section 7.2 of Reference [1] for list of valid channels.
RXCTL-RXPT	0	RXPT is set to 0 if the PHY should seek to acquire a Standard Preamble. When set to 1 the PHY should seek to acquire a Burst Preamble.
RXCTL-RXANT	0.. SupportedDiversity[1:0]	Identifies the receive antenna
RXCTL-PTON	0 1	PTON is ignored for single frame reception
CONTROL-RNGEN	0 1	If RangingSupported = 0 RNGEN is set to 0 If RangingSupported = 1 RNGEN is set to 0 to disable RANGINGTIMER setting RNGEN is set to 1 to enable RANGINGTIMER setting
MPI_CONFIG	0 1	If MPI_CONFIG[1]=0 all receive operations are performed in Single Byte per Cycle mode. If MPI_CONFIG[1]=1 all receive operations are performed in DDR mode.

The reception of a single frame in SDR mode is depicted in Figure 7-13, starting from the READY state. The MAC commands the PHY into RECEIVE state by asserting RX_EN while keeping TX_EN de-asserted. Figure 7-14 demonstrates the reception of a single frame in DDR mode.

When the PHY detects the rising edge of RX_EN, it transitions to RECEIVE state, turns on the radio receive path, waits RxDelay and then starts a preamble acquisition as defined by RXPT using its receive antenna defined in RXANT on the channel defined in RXCHAN. RxDelay is the turn-on time for the radio receive path.

The PHY has full control over data flow during frame reception.

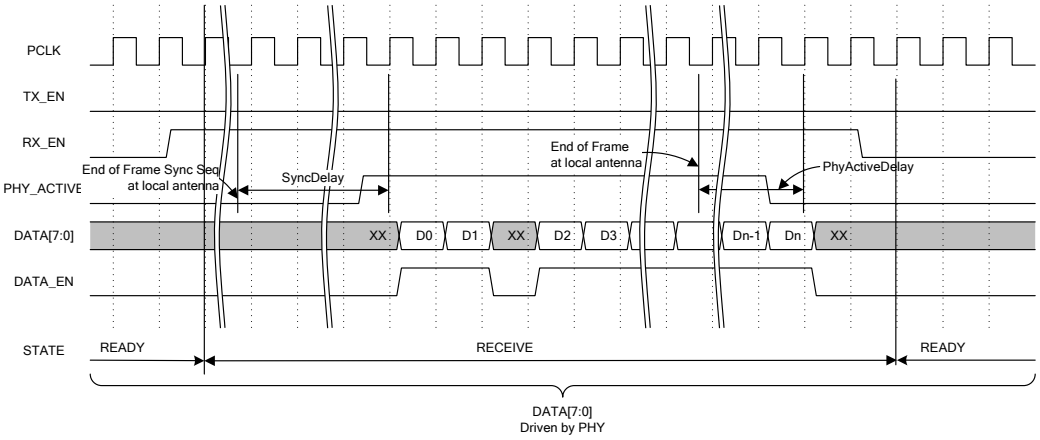


Figure 7-13 Single Frame Receive Timing Diagram SDR mode

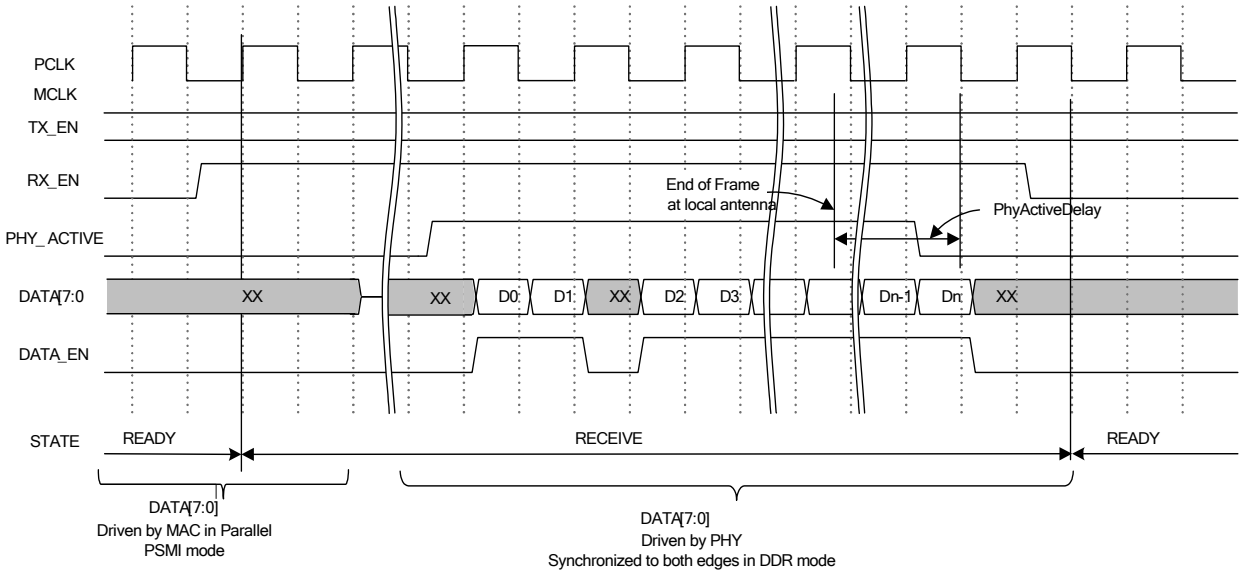


Figure 7-14 Single Frame Receive Timing Diagram DDR mode

The PHY performs the following operations:

- The PHY will seek to acquire the specified preamble on the specified antenna and channel RxDelay after the assertion of RX_EN
- Preamble acquisition is signaled by the PHY asserting PHY_ACTIVE, as indicated in Figure 7-14. The delay between the end of the last symbol of the Frame Synchronization Sequence of the preamble (before the Channel Estimation Sequence) in the antenna and the raising edge of PHY_ACTIVE is a PHY-dependent but fixed delay SyncDelay

- If RNGEN = 1 sets Dynamic Register RANGINGTIMER at the Ranging Reference Signal (defined in the ranging section of Reference [1]) according to the precision defined by the RangingSupported static parameter (see Table 5-1)
- The PHY decodes the received symbols and transfers the PLCP Header to the MAC by the assertion of DATA_EN. In single byte per cycle mode at each PCLK rising edge with DATA_EN asserted the MAC reads one octet of data into the RX Frame. In DDR mode both rising and falling edges of PCLK are used to transfer bytes.
- The PHY interprets the PLCP header parameters and computes the header checksum and compares it with the HCS field in the received PLCP header. The PHY reports the status of the header in HEADER_ERROR as defined in Figure 6-1

The MAC performs the following operations on the RX Frame fields:

- Interprets the HEADER_ERROR parameter. If any bit in HEADER_ERROR is set, the MAC should perform frame recovery by de-asserting and re-asserting RX_EN not less than 3 PCLK cycles later
    - If header checksum verification failed, the receive operation is terminated according to Section 7.11.2.1
    - If the PLCP header RATE is not supported, the PHY terminates the receive operation according to Section 7.11.2.2
- Interprets RX Frame field LENGTH – the length in octets of the MAC Frame Payload. The MAC uses this parameter as needed to support the transfer of received data from the DATA[7:0] bus

The MAC continues the receive operation, if HEADER_ERROR reports no errors. One octet of data is transferred for each rising edge of PCLK while DATA_EN is asserted. In DDR mode there is also one octet of data transferred for each falling edge of PCLK while DATA_EN is asserted. After LENGTH octets have been received the MAC transfers the 4 octets of the FCS and 3 octets of receive quality information into the receive frame and processes the remaining parameters:

- RX Frame field FCS. The MAC computes the FCS according to its specified CRC algorithm and compares the result with the RX Frame FCS value to determine the validity of the MAC Frame Payload data
- RX Frame field RSSI – received signal strength indication. The MAC uses this value as required to support links with the transmitting device
- RX Frame field LQI – link quality indicator. The MAC uses this value as required to support links with the transmitting device
- RX Frame field RXERROR – receive error status. The MAC interprets any set bit in RXERROR as required to perform frame reception error handling

If the PHY had detected an unrecoverable payload error, the receive operation would have been terminated according to 7.11.2.3.

The PHY completes the receive operation by:

- De-asserting PHY_ACTIVE at the rising edge of PCLK a PHY-dependent but fixed delay, PHYActiveDelay, after the trailing edge of the packet waveform at the local antenna

The MAC completes the receive operation by:

- De-asserting RX_EN. The PHY remains in RECEIVE state until RX_EN is de-asserted by the MAC, at which point it transitions back to READY.

A frame reception can be aborted before completion by de-asserting RX_EN as described in section 7.10.

7.8.3 Burst Mode Reception Control

In Burst Mode reception the receiving MAC commands the PHY to perform continuous frame reception by maintaining RX_EN asserted following reception of a frame with BM set to 1. Each frame received with BM = 1 is processed in a manner identical to single frame reception except for the de-assertion of RX_EN to complete the reception operation. The frame symbol timing is determined by the transmitter but the receiving PHY can exploit the PLCP header BM and PT fields to improve receive performance.

There is one receive control register specific to burst mode as shown in Table 7-7.

Table 7-7 Unique Burst Mode Receive Registers

PARAMETER	VALUE	COMMENT
RXCTL-PTON	0	When PTON = 0, the MAC must control all receive preamble acquisition via RXPT
	1	When PTON = 1, the PHY interprets the PT field in PLCP headers with BM = 1

Following reception of a frame with BM = 1 and PT = p, the PHY will prepare to receive a new preamble exactly MIFS after the end of that frame using the preamble indicated by RXPT if PTON = 0, or the preamble indicated by p if PTON = 1.

Figure 7-15 shows a sequence of burst mode received frames with MIFS separation. The timing of each frame is bracketed by the assertion and de-assertion of PHY_ACTIVE with SyncDelay and PhyActiveDelay as in the case of single frame reception.

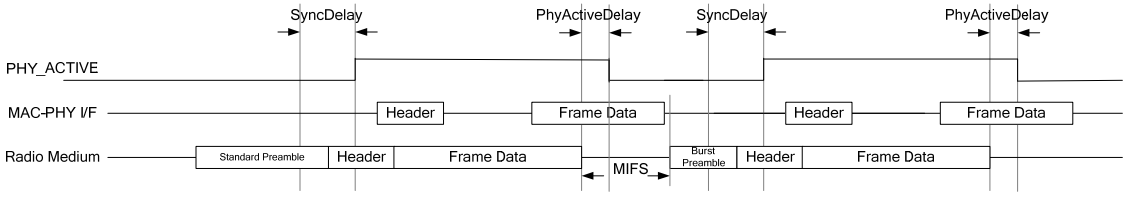


Figure 7-15 Burst Mode Receive with MIFS

As long as each received frame carries BM = 1 the MAC maintains RX_EN asserted and the PHY will continue to perform acquisition and frame reception, each time using the preamble as defined by the previously received PT value or the RXPT value depending on the setting of PTON.

The burst is terminated upon receipt of a frame with BM = 0 after which the MAC de-asserts RX_EN in an identical manner to that for single frame reception.

7.8.4 Burst Mode Reception Error Recovery

At any time within a burst, the MAC may recover from reception errors and terminate Burst Mode reception by de-asserting RX_EN.

7.8.5 Zero-Length Frame Reception

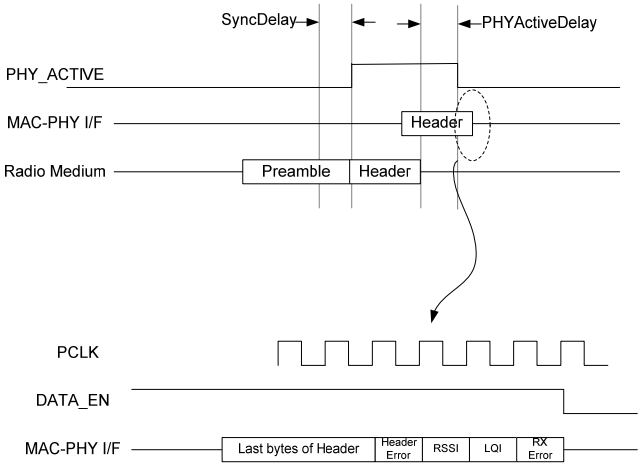


Figure 7-16 Zero Length Frame Reception

Figure 7-16 shows zero length frame reception and presentation of the associated receive parameter block (RSSI, LQI and RXERROR) following the HEADER_ERROR octet.

The receive parameters do not necessarily follow immediately after the HEADER_ERROR octet as the PHY may exploit flow control via DATA_EN when delivering the receive parameter block.

Note that DATA_EN is always used to qualify DATA[7:0] as the PHY retains full flow control during receive operation.

7.9 MAC Transmit Abort

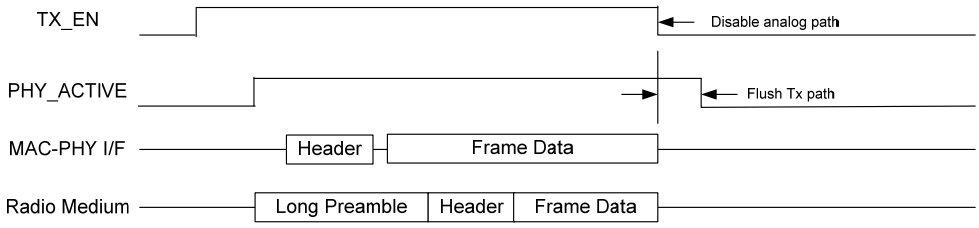


Figure 7-17 MAC Aborted Transmit

Figure 7-17 shows the operation of the interface when the MAC de-asserts TX_EN before delivering the last octet of the FCS to the DATA[7:0] bus.

Upon detecting de-assertion of TX_EN, the PHY should immediately disable the path to the local antenna so that no further symbols are transmitted but may take the necessary time to

flush the transmit logic before de-asserting PHY_ACTIVE at the rising edge of PCLK and returning to READY state.

Note that it is assumed that immediate cessation of transmission at the local antenna is expected to require disabling the analog transmit path. The PHY will normally require additional time to reset the digital transmission path before being ready to resume normal operation.

7.10 MAC Receive Abort

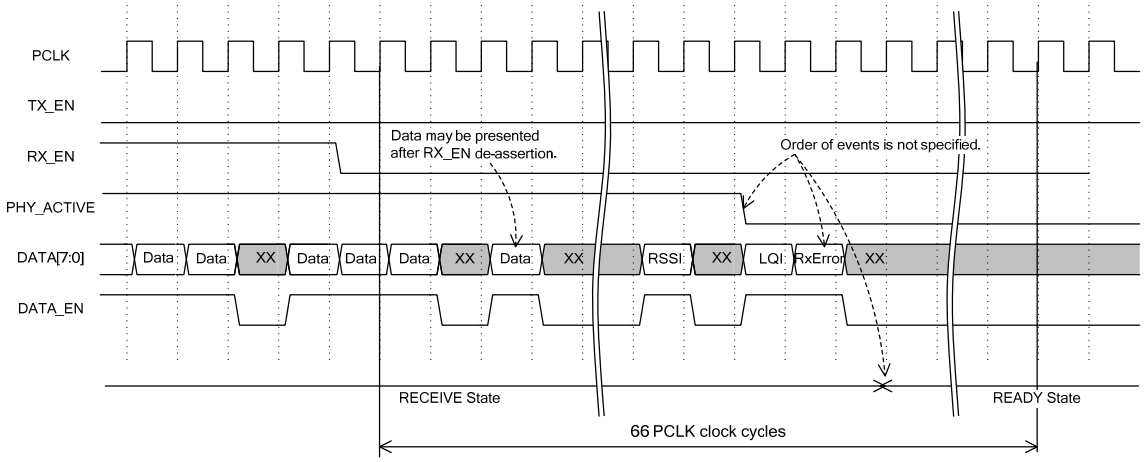


Figure 7-18 MAC Aborted Receive Timing Diagram

Figure 7-18 shows the operation of the interface when the MAC de-asserts RX_EN before the end of frame has been received at the local antenna. Normal RECEIVE operation requires that RX_EN be asserted until after the last octet of the receive parameter block (RXERROR) has been presented to the MAC at the DATA[7:0] bus and validated by DATA_EN.

- The MAC may abort a receive operation at any time after asserting RX_EN by de-asserting RX_EN

If RX_EN is de-asserted at any time before this last octet transfer, irrespective of whether PHY_ACTIVE is asserted or de-asserted, the following abort operation occurs:

- Within 66 PCLK clock cycles of detecting the de-assertion of RX_EN, the PHY shall abort the receive operation, shall stop transferring data to the MAC, shall present the receive parameter block which will be qualified by DATA_EN and shall de-assert PHY_ACTIVE (if asserted)
- If 19 or more octets of data, including the PHY header, the MAC header and HEADER_ERROR have been delivered by the PHY, the MAC shall consider the last three octets delivered by the PHY within these 66 PCLK clock cycles to be the receive parameter block
- Otherwise, all data delivered by the PHY for the aborted receive operation is undefined.

The order in which PHY_ACTIVE is de-asserted and the receive parameter block is presented is not specified but must complete within 66 PCLK cycles after de-assertion of RX_EN.

(A special case should be noted for Burst Mode - if the acquisition of the next frame is signaled by the assertion of PHY_ACTIVE before the completion of delivery of the data and receive quality block of the preceding frame, de-assertion of RX_EN will abort both the delivery of the preceding frame and the incoming frame.)

7.11 Error Conditions

7.11.1 Transmit Error Conditions

There are no defined error conditions that occur during transmit operations.

7.11.2 Receive Error Conditions

7.11.2.1 Header Checksum Error

The PHY computes the header checksum (HCS) for the received PHY Header and compares it with the value in the header HCS field. If this check fails, the contents of the header cannot be trusted – including the critical LENGTH parameter that defines the extent of the MAC Frame Payload field.

In this case, the PHY sets the HEADER_ERROR bits in the receive frame data structure. The PHY then behaves as if a zero length frame had been received.

Even though the header checksum fails to validate the header, the Rx Frame will contain the following:

- The PLCP header including the RATE and LENGTH
- The MAC header
- The HEADER_ERROR bits
- RSSI
- LQI
- RXERROR

The PHY shall de-assert PHY_ACTIVE at a suitable interval after detection of the header checksum failure. In this HCS error case, end of frame timing derived from the de-assertion of PHY_ACTIVE is not valid. HEADER CHECKSUM ERROR is set in both HEADER_ERROR and RXERROR fields.

If the MAC maintains RX_EN asserted following the indication of HCS error, the PHY will continue to seek to acquire a frame using the same preamble type used in the frame whose header checksum failed.

If the Preamble type needs to be re-set (e.g. after failure to acquire a Burst Preamble, the MAC may set the preamble to Standard Preamble) the MAC should de-assert RX_EN, set RXPT to the appropriate value and re-start the PHY's acquisition operation by re-asserting RX_EN. It is the MAC's responsibility to determine the timing of re-acquisition following a lost frame, including loss of an intermediate frame in a burst.

7.11.2.2 Unsupported Data Rate

If the data values in the PHY and MAC Header are validated by the HCS but one or more of the parameters is set to an unsupported value (e.g. Rate), the PHY sets the HEADER_ERROR bits in the receive frame data structure and performs a zero length frame receive operation as described in Section 7.11.2.1.

The PHY shall de-assert PHY_ACTIVE at a suitable interval after detection of the unsupported data rate. The corresponding error bits are set in both the HEADER_ERROR and RXERROR fields.

7.11.2.3 Unrecoverable Detected Payload Error

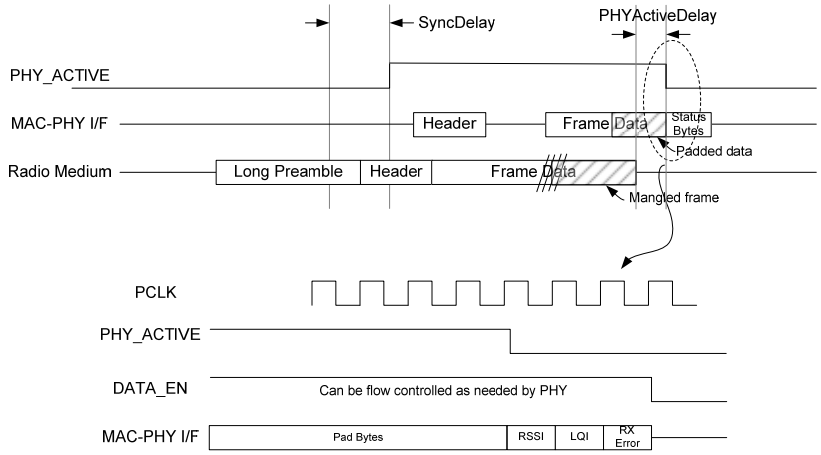


Figure 7-19 Unrecoverable Payload Error Handling

Figure 7-19 shows how an incoming frame aborted by the PHY is signaled after the PHY detects an unrecoverable error while receiving the frame body.

In this case, the PHY can use the content of the PLCP header which has been received with a good HCS. The PHY uses the LENGTH field to determine how many octets of the frame body remain to be transferred to the MAC via the DATA[7:0] bus.

The PHY pads this many undefined value octets at DATA[7:0], qualified by DATA_EN to complete the receive frame operation. PHY_ACTIVE is de-asserted at the nominal end of frame at the local antenna that the PHY computes from LENGTH plus PHYActiveDelay (see Figure 7-19). The receive quality block is transferred as for a normally completed receive operation.

The PHY sets the PAYLOAD_ERROR bit in RXERROR to signal the aborted receive. In addition, the undefined value pad octets will in general cause the MAC FCS check to fail.

7.11.2.4 Wrong Channel

If the data values in the PHY and MAC Header are validated by the HCS but the PLCP Header TxTFC and Band Group LSB bits indicate the frame is transmitted on a different channel to that identified in the RXCHAN register, the PHY sets the WRONG_CHANNEL HEADER_ERROR bit in the receive frame data structure and performs a normal length frame receive operation as described in Section 7.8.

The receiving MAC should interpret the HEADER_ERROR bits and act in a manner appropriate for the MAC implementation. Such actions may be dependent on the value of the PHY_VERSION static parameter (see Appendix B2) and may include normal reception of the frame or Rx Abort (as defined in Section 7.10).

The WRONG_CHANNEL bit is set in both the HEADER_ERROR and RXERROR fields of the receive data structure.

7.12 Clear Channel Assessment

The CCA Interface is used for Clear Channel Assessment status indication. It consists of the CCA_STATUS signal and the following dynamic registers:

Table 7-8 CCA Dynamic Registers

ADDRESS	REGISTER	BIT	FIELD	R/W	DESCRIPTION	INIT.
00(h)	CONTROL	3	CCRE	R/W	The MAC controls CCA estimation by the PHY by writing to CCRE. 0 Stop CCA Estimation 1 Start CCA Estimation	0

Other Dynamic Registers may be provided in the Vendor Specific Register area for enhanced control of the CCA operation since measurement intervals and detection thresholds are highly dependent on the design of the estimation circuit.

7.12.1 CCA Interface Signals

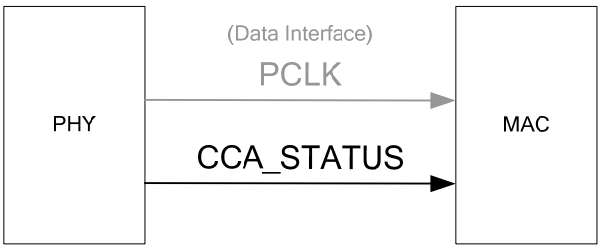


Figure 7-20 CCA Interface Signals

Table 7-9 CCA Interface Signals

SIGNAL NAME	WIDTH	DIRECTION	FUNCTION
CCA_STATUS	1	PHY-MAC	CCA status. 0 indicates that the wireless medium is idle. 1 indicates that the medium is busy.

7.12.2 CCA Interface Operation

The MAC writes a '1' to the CCRE field of the CONTROL register, using the Management Interface, to initiate a CCA measurement.

CCA_STATUS will be driven after PHY-specific but constant interval CCAValidTime according to the implementation-dependent CCA estimation algorithm, and will be valid as long as the PHY is not in TRANSMIT, STANDBY or SLEEP state. Estimation will continue as long as CCRE is set to 1.

The MAC writes 0 to CCRE, using the Management Interface, when CCA estimation is no longer required.

All other CCA operations will depend on vendor-specific register settings.

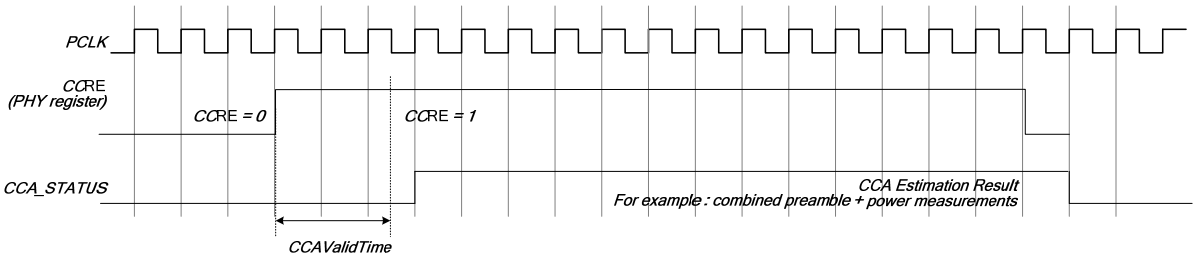


Figure 7-21 CCA Operating Timing Diagram

7.13 Management Interface

7.13.1 Management Interface Signals

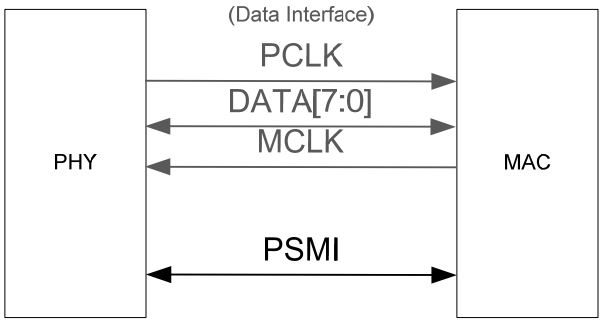


Figure 7-22 Management Interface Signals

Table 7-10 Management Interface Signal Definitions

SIGNAL	DIRECTION	DESCRIPTION
PSMI	MAC to PHY	For serial write operations, the MAC drives register address and register data to the PHY. For parallel write operations, the MAC drives address enables to control the DATA bus.
	PHY to MAC	For serial read operation, the MAC drives register address to the PHY. The PHY drives register data to the MAC. For parallel read operations, the MAC drives an address enable and the PHY drives a data enable.
MCLK	MAC to PHY	Clock sourced by the MAC. PSMI and DATA are synchronous to this clock during ADDRESS phase and data WRITE phase.
PCLK	PHY to MAC	Clock sourced by the PHY. PSMI and DATA are synchronous to this clock during data READ phase.
DATA[7:0]	Bi-Directional	Data bus available to Management Interface when not in Transmit or Receive state. Used in Parallel Management mode to load address and data.
Note. It is the responsibility of the MAC to ensure the PSMI signal is driven to the '0' level except during READ or WRITE operations.		

7.13.2 Management Interface Operation

The Management interface is used by the MAC to read/write control registers in the PHY. It has two modes of operation: serial and parallel.

Serial Management Interface mode uses only the PSMI signal to transfer address and data in a serial fashion. Default operation assumes serial mode.

Parallel Management Interface mode uses the PSMI signal as a control signal and the address and data is loaded in parallel on the DATA bus. The Management Interface is placed in parallel mode by setting the dynamic MPI CONFIG register appropriately. The DATA bus is shared with the Transmit and Receive operations. When in TX or RX mode the DATA bus is not available for the Management Interface to use. In this case the Management Interface has to fall back to serial mode. The operation of the PSMI is

independent of the SDR/DDR setting of the DATA bus as controlled by MPI CONFIG register bit 1. When the DATA bus is in DDR mode the PSMI interface continues to use only the rising edge of the clocks to operate.

MCLK shall be enabled during the Address and data WRITE phase of the Management Interface operation. It may operate during other periods but shall not be required.

The DATA bus in Serial Management Mode shall be driven by the PHY in all states except Transmit state. When the management interface is switched to Parallel Management Mode a switch is made where the MAC shall drive the DATA bus in all states except Receive state. There are several requirements to establish proper ownership of the DATA bus in parallel mode. They are:

- A new state is introduced called RX_EN_FINISH defined as the 66 PCLK cycles following the falling edge of RX_EN. This is the time the PHY is permitted to finish an aborted RECEIVE operation as defined in section 7.10. RX_EN_FINISH state shall be aborted if TX_EN is asserted. RX_EN_FINISH state is only active when the PSMI interface is placed in parallel mode. Its use is to coordinate the DATA bus tri-state control and is initiated at the completion of both normal and aborted RECEIVE states.
- In parallel PSMI mode the MAC drives the DATA bus except in RECEIVE and RX_EN_FINISH states.
- In parallel PSMI mode the Management interface shall not initiate a read or write operation during the 4 cycles following the de-assertion of TX_EN or RX_EN_FINISH.

7.13.2.1 Read Operation Serial Mode

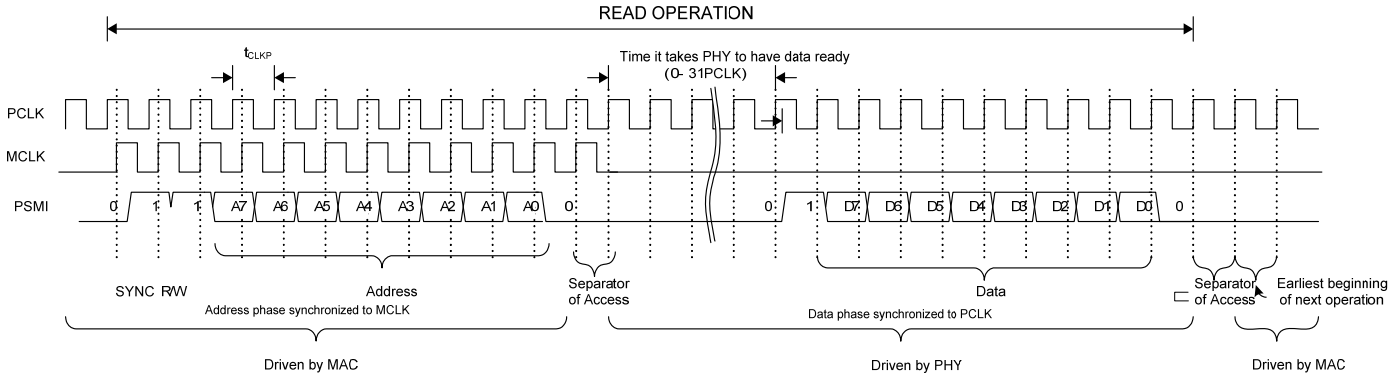


Figure 7-23 Serial Read Operation

For a serial read operation, the MAC drives the first part of the transaction, which includes the PHY register address. The PHY drives the second part of the transaction, which includes the requested data. The first part of the transaction driven by the MAC is synchronized with MCLK. The data portion driven by the PHY is synchronized with PCLK.

The MAC will drive a “1” as the first bit on the PSMI pin. The second bit is a “1”, which indicates a read operation. The MAC drives the next 8 bits, which are the PHY register address. This allows the MAC to address up to 256 PHY configuration registers. After the 8-bit address, the MAC drives a ‘0’ bit to place the PSMI line in a known state.

The PHY drives ‘0’ to the PSMI line for a period from 0 to 31 PCLK cycles beginning on the second PCLK after the MAC stops driving the interface.

The PHY drives a ‘1’ bit to indicate start of data followed by 8 data bits. The transaction is completed by driving a terminating ‘0’ bit to place the PSMI line in a known state before releasing the line to be driven by the MAC. Figure 7-24 shows the timing for the fastest PHY response to a read operation.

(Note: Implementer can use internal or external pull-down resistors to set the PSMI pin to 0 when the MAC is no longer driving the signal.) The MAC will resume control of the PSMI pin.

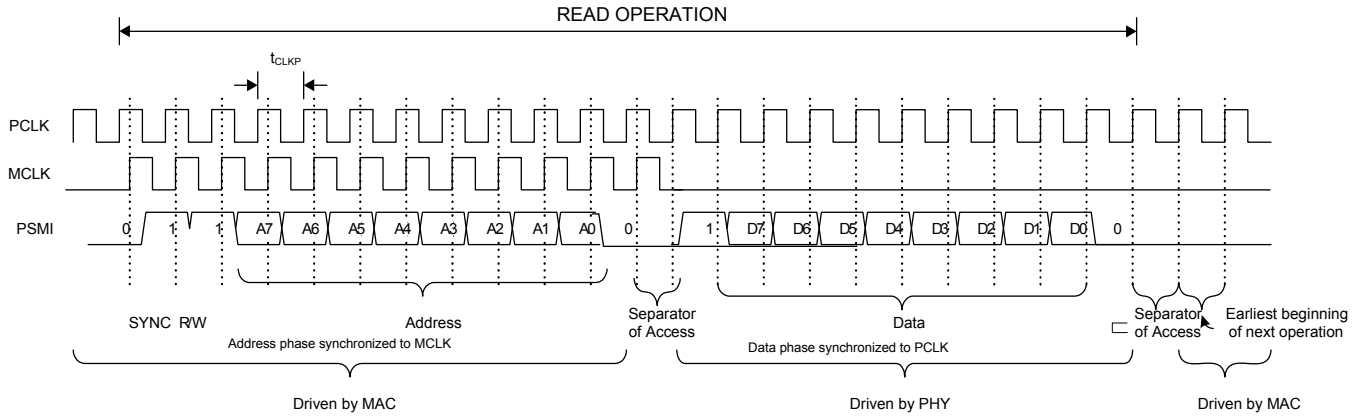


Figure 7-24 Fastest Read Response

7.13.2.2 Write Operation Serial Mode

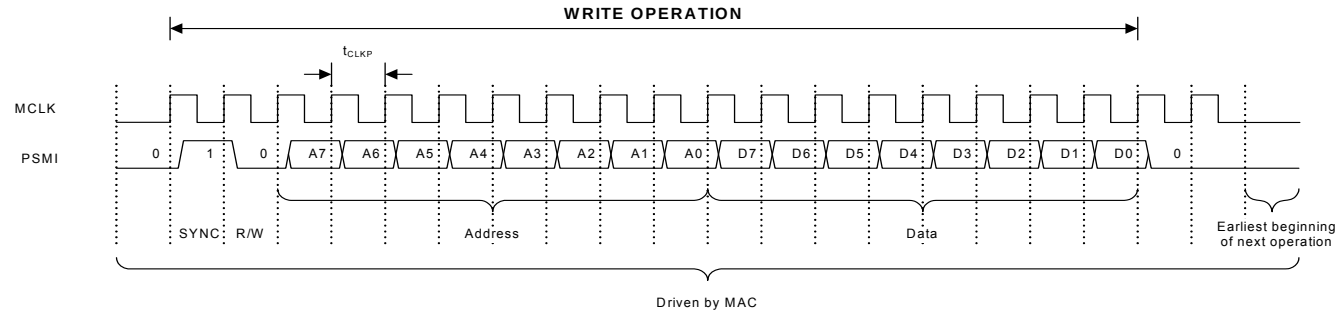


Figure 7-25 Serial Write Operation

For a serial write operation, the MAC drives the entire transaction. Each bit the MAC drives on the PSMI pin is synchronized with MCLK.

The MAC will drive a “1” as the first bit on the PSMI pin. The second bit is a “0”, which indicates a write operation. The next 8 bits are the PHY address location. This allows the MAC to address up to 256 octets of PHY configuration registers. The next 8 bits are the data to be written to the addressed PHY register. At the end of 8 bits of data, the MAC will

drive a terminating “0.” Once the transaction is complete the MAC stops driving the management interface.

(Note: Implementer can use internal or external pull-down resistors to set the PSMI pin to 0 when the MAC is no longer driving the signal.) The PSMI pin will continue to be controlled by the MAC. Figure 7-26 shows the fastest timing for a read operation followed immediately by a write operation in serial management mode.

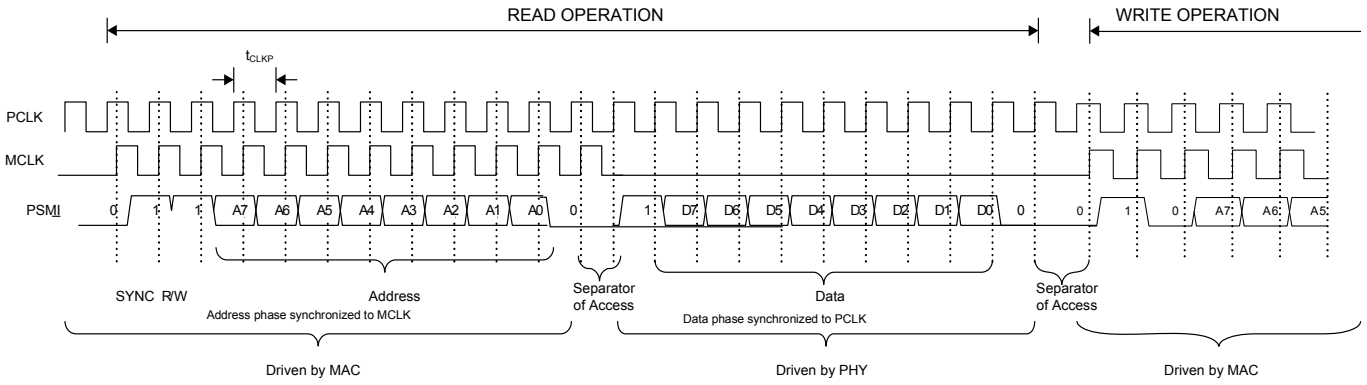


Figure 7-26 Read Operation Followed By Write Operation

7.13.3 Read Operation Parallel Mode

Parallel operation is much like serial operation except the address and data bits are loaded in parallel on the DATA bus instead of shifting serially on the PSMI signal. In Parallel PSMI read mode the DATA bus is initially driven by the MAC for address phase. Once a Parallel Read Data phase has been started the DATA bus switches to be driven by the PHY until the read data is loaded. MCLK only needs to run during the address portion of the transactions.

Also shown are the signals that control the selection of serial vs. parallel mode. For the 4 cycles following the de-assertion of TX_EN or RX_EN_FINISH the MAC shall not initiate a transaction. The parallel read can take up to 31 cycles for the PHY to respond with the parallel data. If TX_EN or RX_EN are asserted at any time before the read is complete it shall abort.

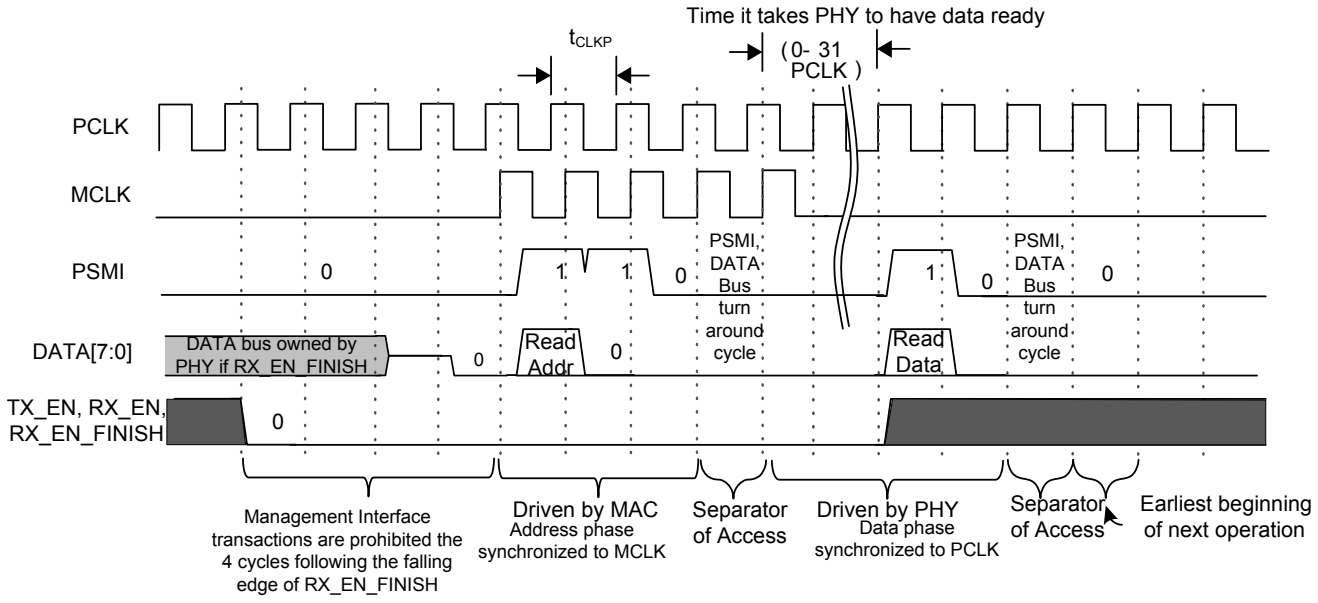


Figure 7-27 Parallel Read Operation

7.13.4 Write Operation Parallel Mode

Parallel write operations only require 2 clock cycles per byte. Figure 4-1 shows three back-to-back parallel write operations. MCLK only needs to run during the transactions. Also shown are the signals that control the selection of serial vs. parallel mode. There are at least four cycles following the end of TX_EN, RX_EN, or RX_EN_FINISH that the MAC is prohibited from initiating a transaction. Once a parallel write has begun by asserting PSMI, it shall complete without aborting.

Back-to-back parallel write operations or parallel write followed by a parallel read operation may or may not have delay(s) between the operations depending on the MAC functionality.

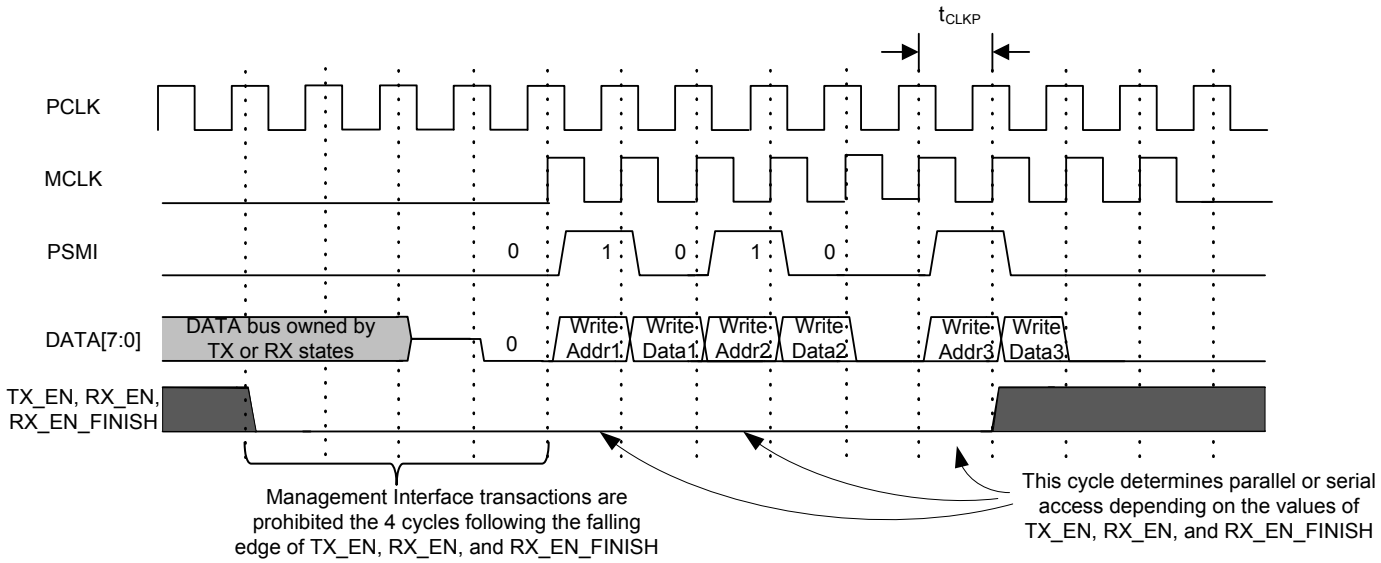


Figure 7-28 Parallel Write Operation

7.13.5 Management Parallel/Serial Switching

The DATA bus is owned primarily by the RECEIVE and TRANSMIT states. The Management interface shall release the DATA bus immediately in order not to impede the normal data transfer operations.

There are 3 conditions that indicate the DATA bus is busy: 1) the assertion of RX_EN, 2) the assertion of TX_EN, and 3) the assertion of the internal RX_EN_FINISH state.

RX_EN_FINISH state is defined as the 66 clock cycles following the de-assertion of RX_EN. The Management Interface logic for both the MAC and PHY shall generate this state to aid in the ownership of the DATA bus. The purpose of RX_EN_FINISH is to account for normal RECEIVE finish and the possibility of a RECEIVE ABORT. Section 7.10 defines the requirement for this signal. During the RX_EN_FINISH period it is unknown by the Management Interface if the DATA bus has been released. It is therefore assumed to be busy. RX_EN_FINISH is an extension of the RECEIVE state which means the PHY shall own the bus during this period. The 4 cycles following the de-assertion of RX_EN_FINISH are used to turn around the data bus.

The RX_EN_FINISH counters in the MAC and PHY are on different clock domains. It is possible they are not exactly synchronized. Because of this the exact cycle the DATA bus switches from PHY to MAC may not be precise. To prevent serial/parallel mode ambiguity the MAC should not initiate a transaction during the 5 cycles following the de-assertion of RX_EN_FINISH. This safety cushion of one cycle beyond the required spec is desirable but not required to maintain a robust synchronized Management Mode.

Parallel write operations only take 2 clock cycles. Once a write has begun it shall finish. Data bus tri-state controls are defined in such a way that the write operation cannot interfere with Transmit or Receive.

A parallel read operation may take up to 38 cycles. If during a parallel read the DATA bus is requested by assertion of TX_EN or RX_EN, the read operation shall immediately abort the parallel operation and release the DATA bus.

Serial read and write operations, once started, shall complete in serial mode.

Figure 7-29 shows a parallel read operation that has been aborted. Note that the PHY does not assert the PSMI signal to indicate the read data is ready. Instead, two cycles after the assertion or TX_EN or RX_EN the PHY releases the DATA bus to the RECEIVE or TRANSMIT state machine.

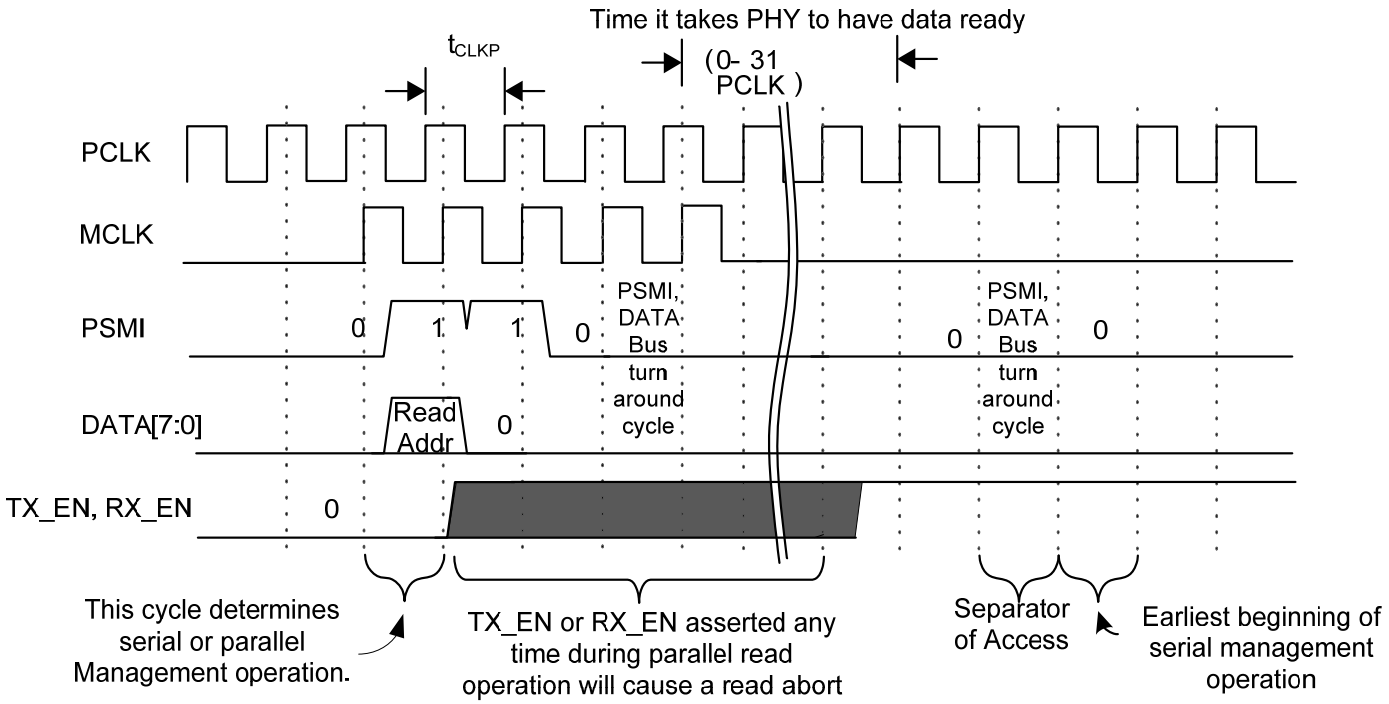


Figure 7-29 Parallel Read Abort

7.13.6 Examples

7.13.6.1 Serial read Operation Example

The MAC wants to read the PHYID (addresses 0x20h and 0x21h). PHYID is 1B86 hex stored in big-endian representation. In this example it takes the PHY four clock cycles to have the data available.

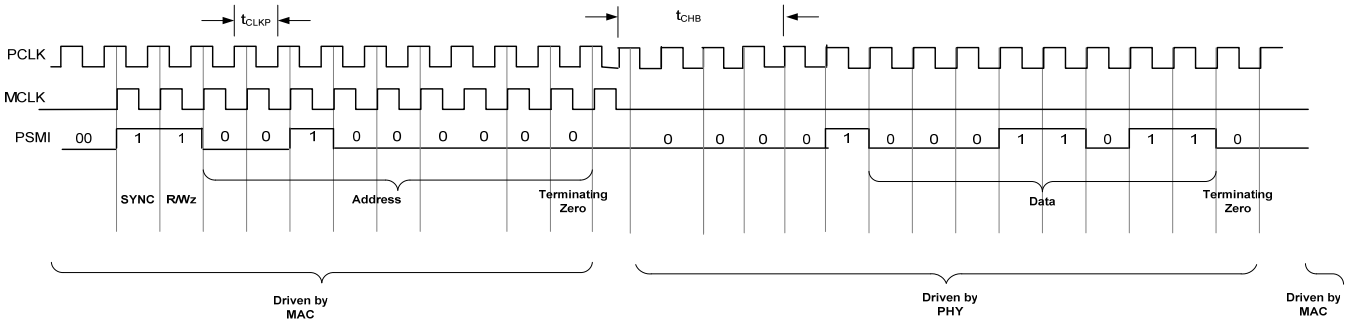


Figure 7-30 Serial Read Example, Address 20hex

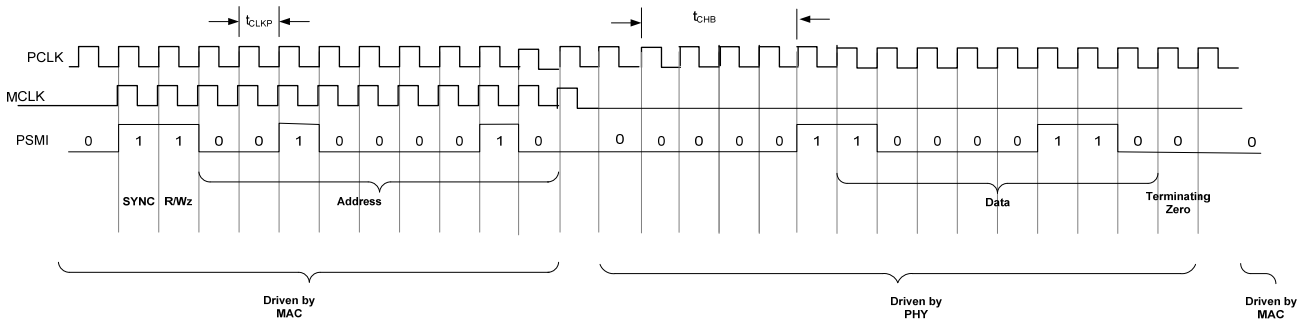


Figure 7-31 Serial Read Example, Address 21hex

7.13.6.2 Serial Write Operation Example

MAC wants to put PHY into READY state by setting PMMODE=0. (PMMODE address is 06, READY State is value 0.)

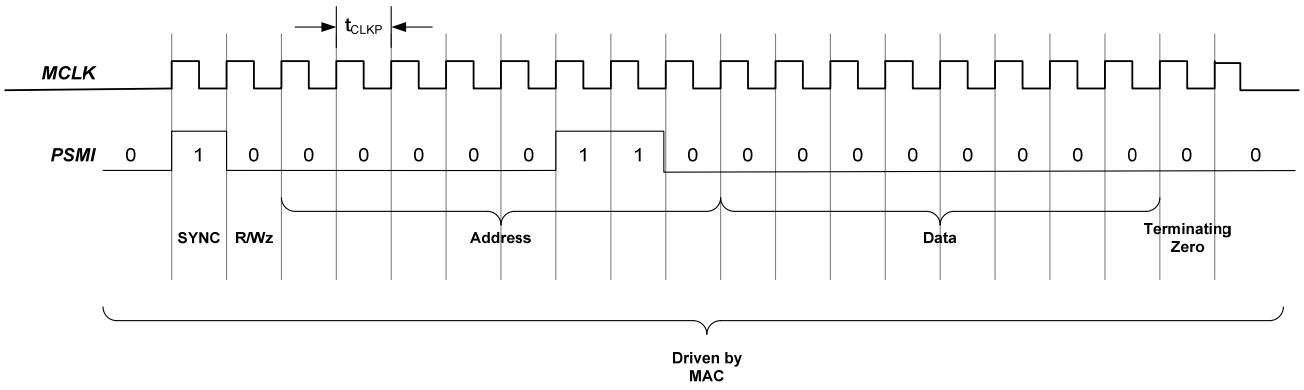


Figure 7-32 Serial Write Example Address 06 hex

7.13.6.3 Parallel and Serial Write Operation Example

This example shows two write operations back-to-back as close together as possible. TX_EN has been toggled to show how the parallel write operation can complete when the DATA bus is requested in the middle of the transaction. The second write transaction shows TX_EN enabled during the first cycle which determines the transfer is to be in serial mode. It also demonstrates that once a serial transfer is started it finishes in that mode.

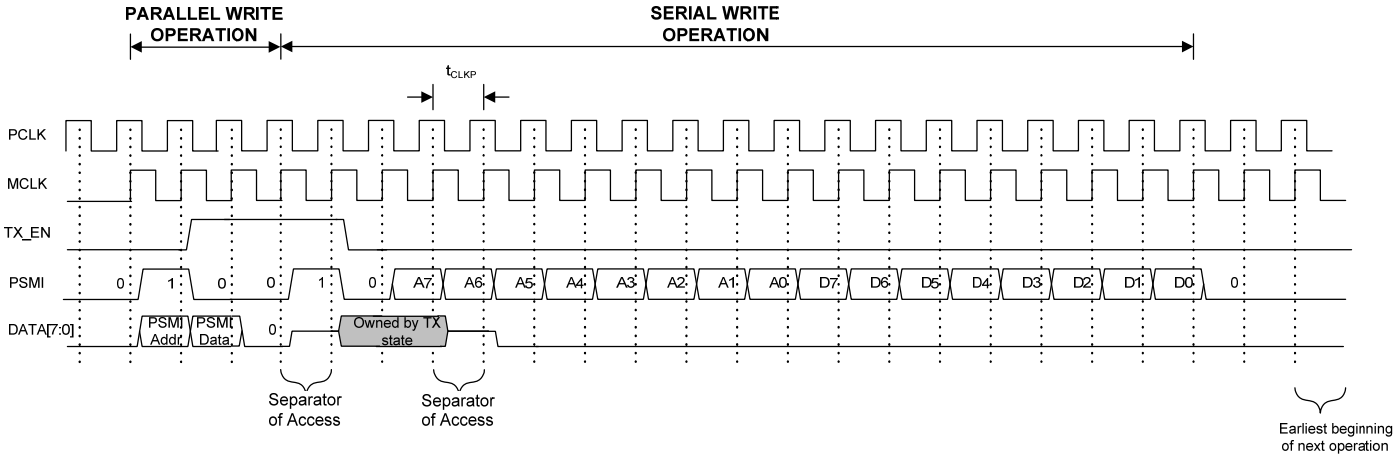


Figure 7-33 Parallel and Serial Write Example

7.13.6.4 Parallel Read Abort and Serial Reissue Worst Case Example

This example is shown in Figure 7-34 Parallel Read Abort and Serial Reissue Example. It shows the worst case response time of an aborted parallel read followed immediately by a reissued serial read. In this case it takes 90 clock cycles to complete the read.

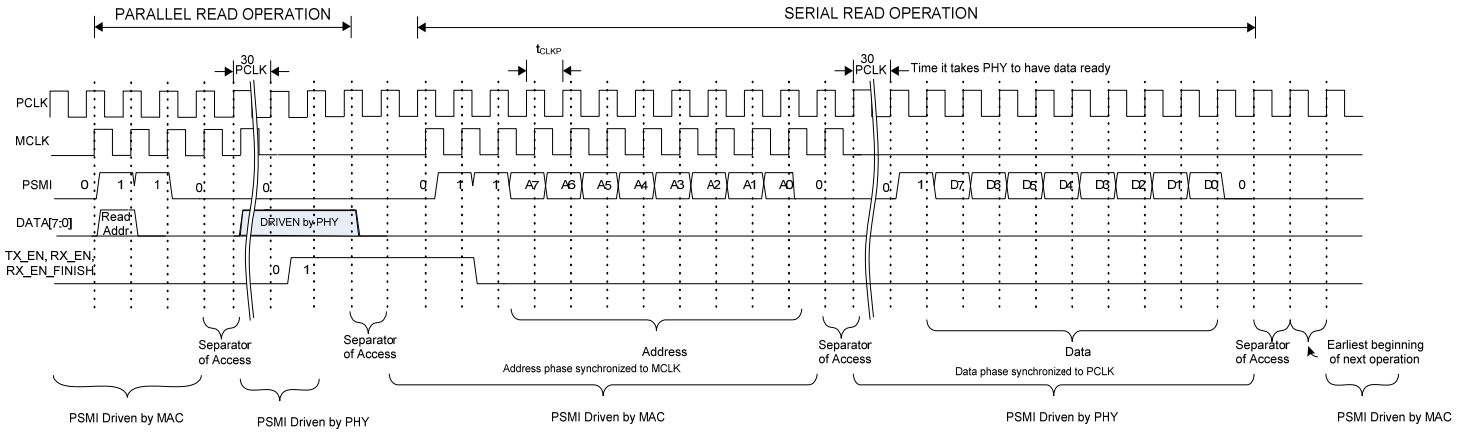


Figure 7-34 Parallel Read Abort and Serial Reissue Example

Appendix A Electrical Specifications

A.1 I/O DC Requirements

To improve interoperability between MAC and PHY implementations by different vendors, the following voltage parameters are recommended:

A.1.1 3.3V DC Specification

Appendix Table A-1 gives the operating range under nominal parameter values:

- Vcc = 3.0V to 3.6V
- Ambient Temperature = 0^0C to 70^0C

Appendix Table A-1 3.3V Functional Operating Range

	PARAMETER	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS	NOTES
	V_{CC}	Supply Voltage		3.0	3.6	V	
INPUT	V_{IH}	Input high voltage		2	Vcc+0.5	V	1
	V_{IL}	Input low voltage		-0.3	0.8	V	1
	I_{IL}	Input leakage current	0 < Vin < Vcc	-10	+10	uA	2, 3
	C_{IN}	Input pin capacitance			10	pF	
OUTPUT	V_{OH}	Output high voltage	Iout = -4mA	2.4		V	2
	V_{OL}	Output low voltage	Iout = 4mA		0.4	V	2

A.1.2 1.8V DC Specification

Appendix Table A-2 gives the Operating Range under nominal parameter values:

- Vcc = 1.65V to 1.95V
- Ambient Temperature = 0^0C to 70^0C

Appendix Table A-2 1.8V Functional Operating Range

	PARAMETER	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS	NOTES
	V_{CC}	Supply Voltage		1.65	1.95	V	
INPUT	V_{IH}	Input high voltage		1.2	V_{CC}+0.2	V	1
	V_{IL}	Input low voltage		-0.2	0.7	V	1
	I_{IL}	Input leakage current	0 < Vin < Vcc	-600	+600	uA	2, 3
	C_{IN}	Input pin capacitance			2	pF	
OUTPUT	V_{OH}	Output high voltage	Iout = -4mA	0.8* V_{CC}	V_{CC}	V	2
	V_{OL}	Output low voltage	Iout = 4mA	0	0.2* V_{CC}	V	2

A.1.3 1.2V DC Specification

Appendix Table A-3 gives the Operating Range under nominal parameter values:

- Vcc = 1.1V to 1.3V
- Ambient Temperature = 0^0C to 70^0C

Appendix Table A-3 1.2V Functional Operating Range

	PARAMETER	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS	NOTES
	V_{CC}	Supply Voltage		1.1	1.3	V	
INPUT	V_{IH}	Input high voltage		0.8	V_{CC} +0.2	V	1
	V_{IL}	Input low voltage		-0.2	0.4	V	1
	I_{IL}	Input leakage current	0 < Vin < Vcc	-120	+120	uA	2, 3
	C_{IN}	Input pin capacitance			2	pF	
OUTPUT	V_{OH}	Output high voltage	Iout = -4mA	0.7* V_{CC}	V_{CC}	V	2
	V_{OL}	Output low voltage	Iout = 4mA	0	0.3* V_{CC}	V	2

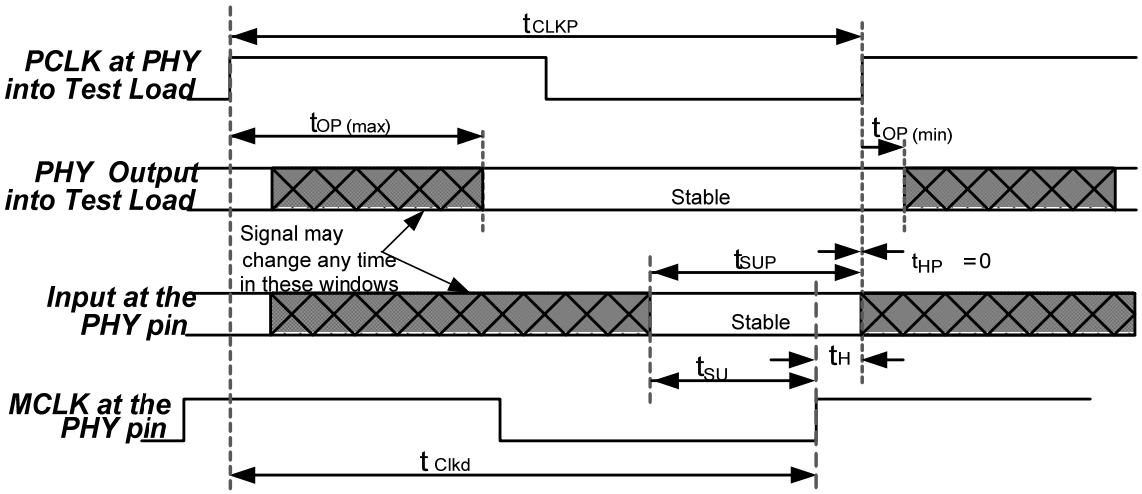
Notes:

1. This is a DC specification. During transitions the inputs may experience overshoot beyond V_{IH}(max) and undershoot below V_{IL}(min).
2. Positive current is defined into the pin.
3. Input leakage currents include Hi-Z outputs leakage for bi-directional buffers with tri-state outputs.

A.2 MAC PHY Timing Specifications

A.2.1 PHY Signal Timings

To improve interoperability between MACs and PHYs from different vendors the following timings for synchronous signals at the PHY are recommended:



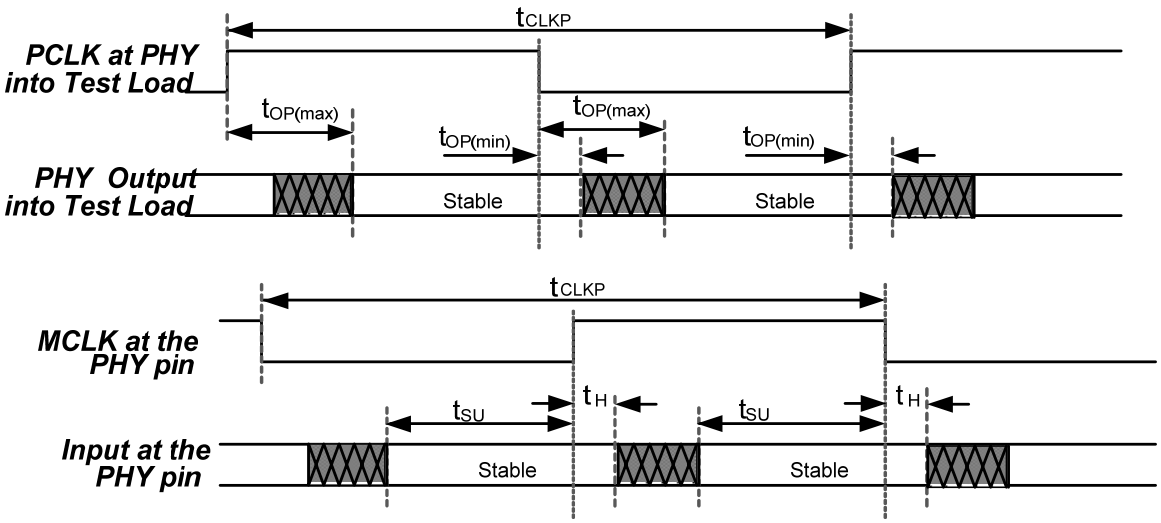
Appendix Figure A-1 PHY Signal Timing Diagram

Appendix Figure A-1 shows the signal timings for the PHY in single data rate mode. Both input and output timings are specified with respect to rising edge of PCLK driven into the specified test load of 10pF crossing V_{meas} = 1.4V. The input timings are also specified with respect to the MCLK input. Input specifications with respect to PCLK are only required to make the interface backward compatible with MPI interfaces earlier than 1.5.

Output timings are specified with the PHY pins driven into the specified test load of 10pF, and are measured at V_{meas} = 1.4V.

Input timings are specified at the PHY pin to V_{IL}(max) for a logic 0 and V_{IH}(min) for logic 1.

All output transitions, in single data rate mode are synchronous with the rising edge of PCLK. All input transitions in single data rate mode are synchronous with the rising edge of MCLK.



Appendix Figure A-2 PHY DDR Signal Timing Diagram

Appendix Figure A-2 shows the signal timings for the PHY in Double Data Rate Mode. Output timings are specified with respect to both rising and falling edges of PCLK driven into the specified test load of 10pF crossing V_{meas} = 1.4V. The input timings are specified with respect to both the rising and falling edges of the MCLK input.

Output timings are specified with the PHY pins driven into the specified test load of 10pF, and are measured at V_{meas} = 1.4V.

Input timings are specified at the PHY pin to V_{IL}(max) for a logic 0 and V_{IH}(min) for logic 1.

All output transitions, in DDR mode are synchronous with the rising and falling edges of PCLK. All input transitions in DDR mode are synchronous with the rising and falling edges of MCLK.

MCLK is defined as having the same frequency as PCLK. However, there is no specified timing relationship between the MCLK domain and the PCLK domain in DDR mode. Note this is not actually true to maintain backward compatibility in single data rate mode.

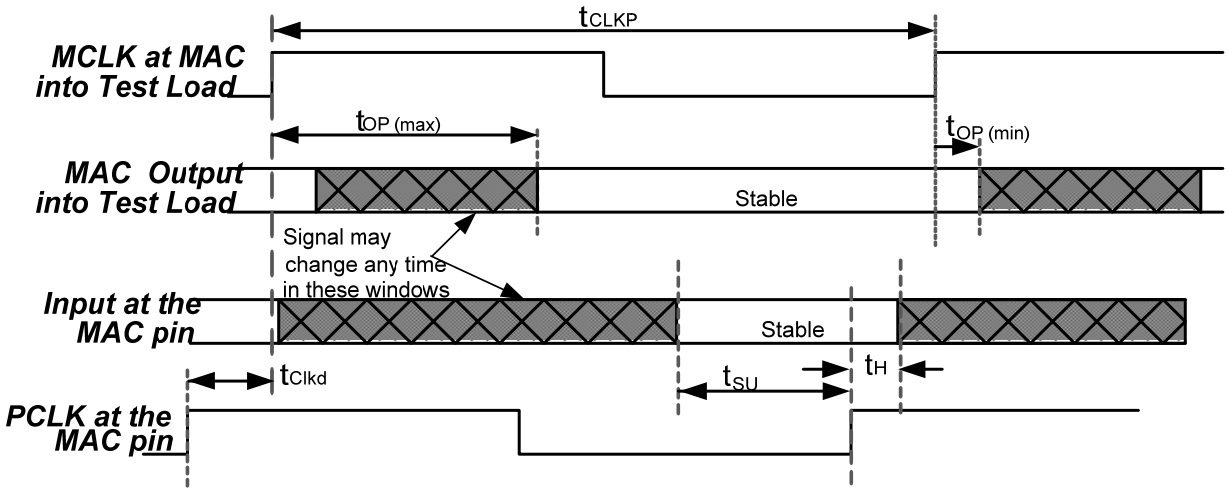
Appendix Table A-4 defines the values for the PHY timing requirements.

Appendix Table A-4 PHY Signal Timing Values

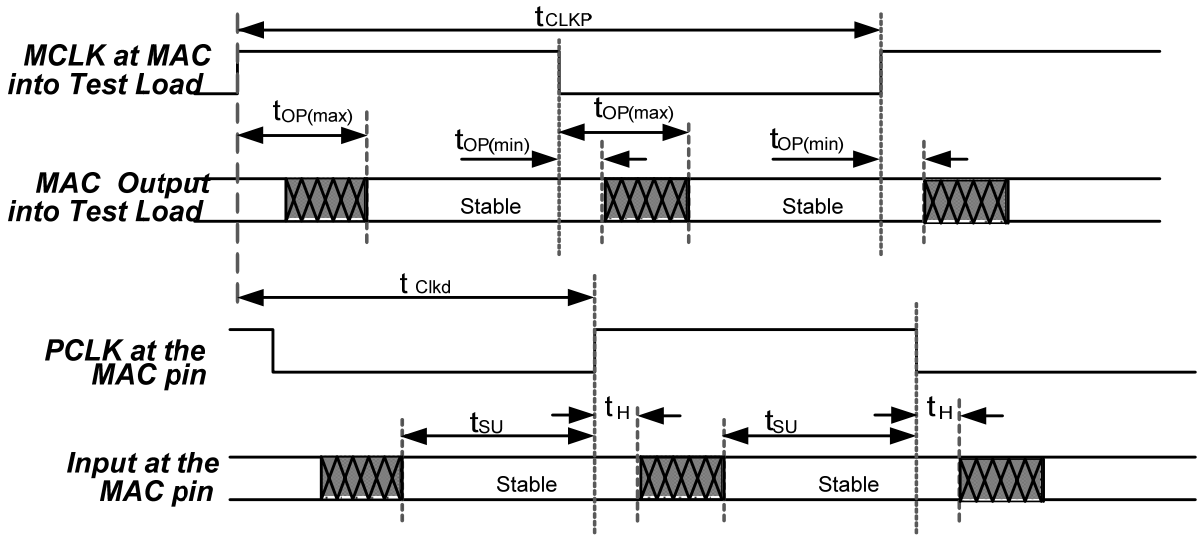
VALUE	DESCRIPTION	MAX	MIN
t_{CLKP}	PHY Clock Period	-	15ns
top	Time PHY output data is valid after the edge of PCLK (nominally ¼ tclkp)	4ns	1ns
t_{SU}	Setup time, to rising edge of MCLK	-	3ns
t_{H}	Hold time, from rising edge of MCLK	-	0ns
t_{SUP}	Setup time, to rising edge of PCLK to maintain backwards compatibility	-	5ns
t_{HP}	Hold time, from rising edge of PCLK to maintain backwards compatibility	-	0ns
t_{CLKd}	Delay from PCLK edge to MCLK edge. This number is used to maintain backward compatibility.	6ns	1ns

A.2.2 MAC Signal Timings

To improve interoperability between MACs and PHYs from different vendors the following timings for synchronous signals at the MAC are recommended:



Appendix Figure A-3 MAC Signal Timing Diagram



Appendix Figure A-4 MAC DDR Signal Timing Diagram

Appendix Figure A-4 shows the signal timings for the MAC in single data rate mode. Input timings are specified with respect to rising edge of PCLK at the MAC pin crossing V_{meas} = 1.4V. The output timings

are specified with respect to the MCLK output. The MCLK specification with respect to PCLK is only required to make the interface backward compatible with MPI interfaces earlier than 1.5.

Output timings are specified with the MAC pin driven into the specified test load of 10pF, and are measured at V_{meas} = 1.4V.

Input timings are specified at the MAC pin to V_{IL}(max) for a logic 0 and V_{IH}(min) for logic 1.

All output transitions, in single data rate mode are synchronous with the rising edge of MCLK. All input transitions in single data rate mode are synchronous with the rising edge of PCLK. In DDR mode both rising and falling edges of the clock are referenced.

Appendix Table A-5 defines the values for the MAC signal timing requirements.

Appendix Table A-5 MAC Signal Timing Values

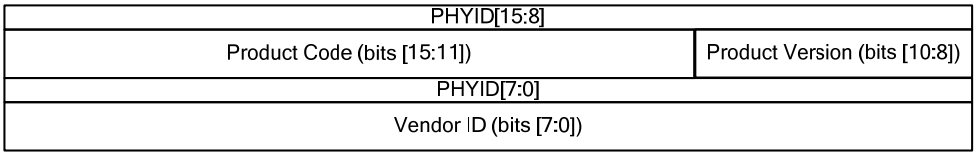
VALUE	DESCRIPTION	MAX	MIN
t_{CLKP}	PHY Clock Period	-	15ns
t_{OP}	Time MAC output data is valid from the rising edge of MCLK	4ns	1ns
t_{SU}	Setup time, to rising edge of PCLK	-	3ns
t_{H}	Hold time, from rising edge of PCLK	-	0ns
t_{CLKd}	Delay from PCLK edge to MCLK edge. This number is used to maintain backward compatibility.	6ns	1ns

Appendix B PHY Vendor and Version Coding

The static parameters defined in Section 5.3 include two PHY identification parameters – PHYID and PHYVersion. The format and coding of these two variables is defined below. Management of the allocation of values to Vendor ID is under the control of the WiMedia Alliance Inc.

B.1 PHYID Format and Coding

Appendix Figure B-1 shows the format of the PHYID parameter.



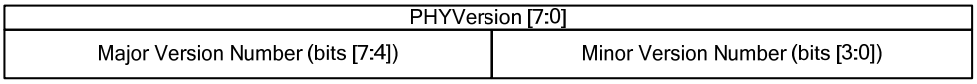
Appendix Figure B-1 PHYID Format

The first octet of PHYID is the Vendor ID field. This field is maintained by the WiMedia Alliance Inc. in Reference [3].

The second octet of PHYID contains a 5-bit product code and a 3-bit product version number. The coding of these two fields is vendor-specific.

B.2 PHYVersion Format and Coding

Appendix Figure B-2 shows the format of the PHYVersion parameter.



Appendix Figure B-2 PHYVersion Format

The PHYVersion parameter contains a 4-bit major version number and a 4-bit minor version number, and declares the version of the WiMedia Multiband OFDM PHY specification to which the PHY implementation complies. The version numbers are maintained by the WiMedia Alliance Inc.

Appendix C Backward Compatibility

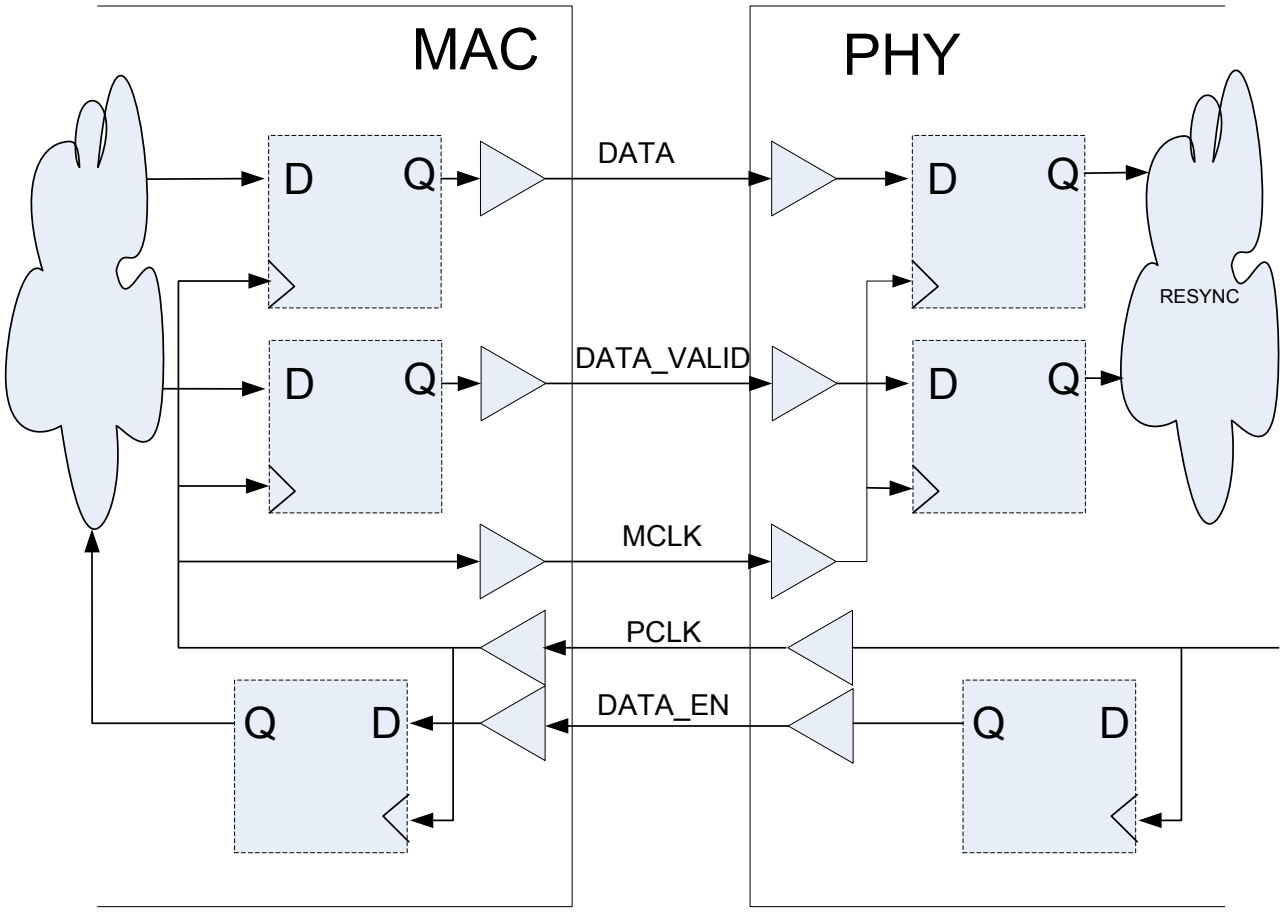
The present revision of the MAC-PHY Interface specification is designed to be backward compatible. Specifically, a PHY (MAC) implementing an older revision of this interface will be able to mate with a MAC (PHY) implementing this revision of the interface, as long as the following guidelines are followed. Figure C-1 shows the register pipelining that is assumed with MPI version 1.2 and earlier. To maintain backward compatibility with the older versions this pipelining must be maintained as shown in figure C-1.

C.1 PHY Implementing MPI 1.5, MAC Implementing Older MPI

In this case, the PHY can mate with the MAC by self-generating the MCLK and DATA_VALID signals. MCLK is generated simply by connecting PCLK to MCLK external to the chip. DATA_VALID must be generated internally and resynchronized with MCLK.

C.2 MAC Implementing MPI 1.5, PHY Implementing Older MPI

In this case the MAC can mate with the PHY by maintaining the proper pipelining for generation of the TX data. Appendix Figure C-1 shows the pipelining of the MAC-PHY interface. If the MAC maintains the relationship between the input DATA_EN and the DATA output the PHY interface will work without using DATA_VALID.



Appendix Figure C-1 Pipelining of MPI